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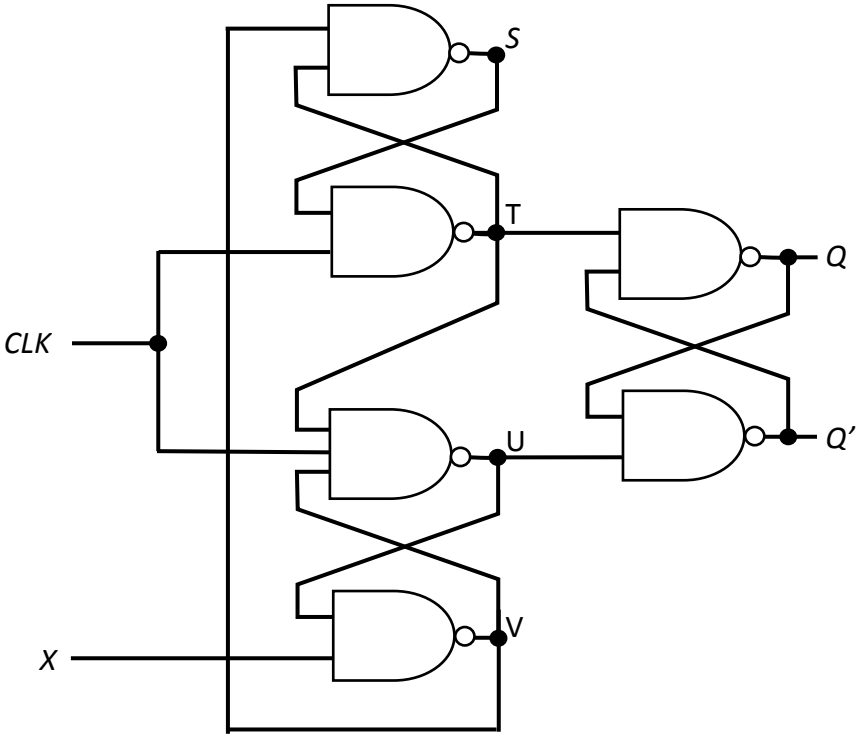
Logic design (2016 fall)

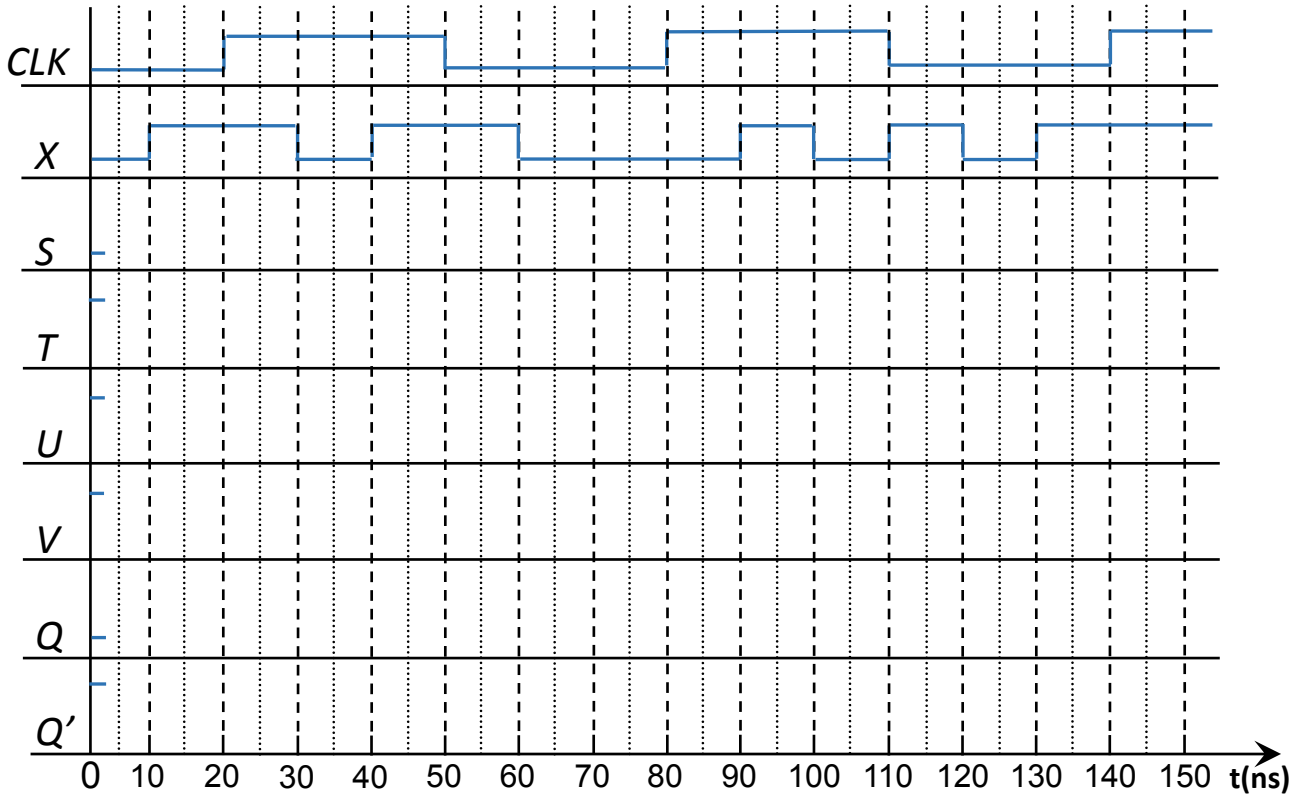
Quiz # 11

Name:_____ID:_____

1. (100%) The *X* flip-flop with three *S*-*R* latches is as follows.



(a) (64%) Complete the following timing diagram, if initially $S = Q = 0$ and $T = U = V = Q' = 1$. Note that each NAND gate has the same propagation delay 5ns.



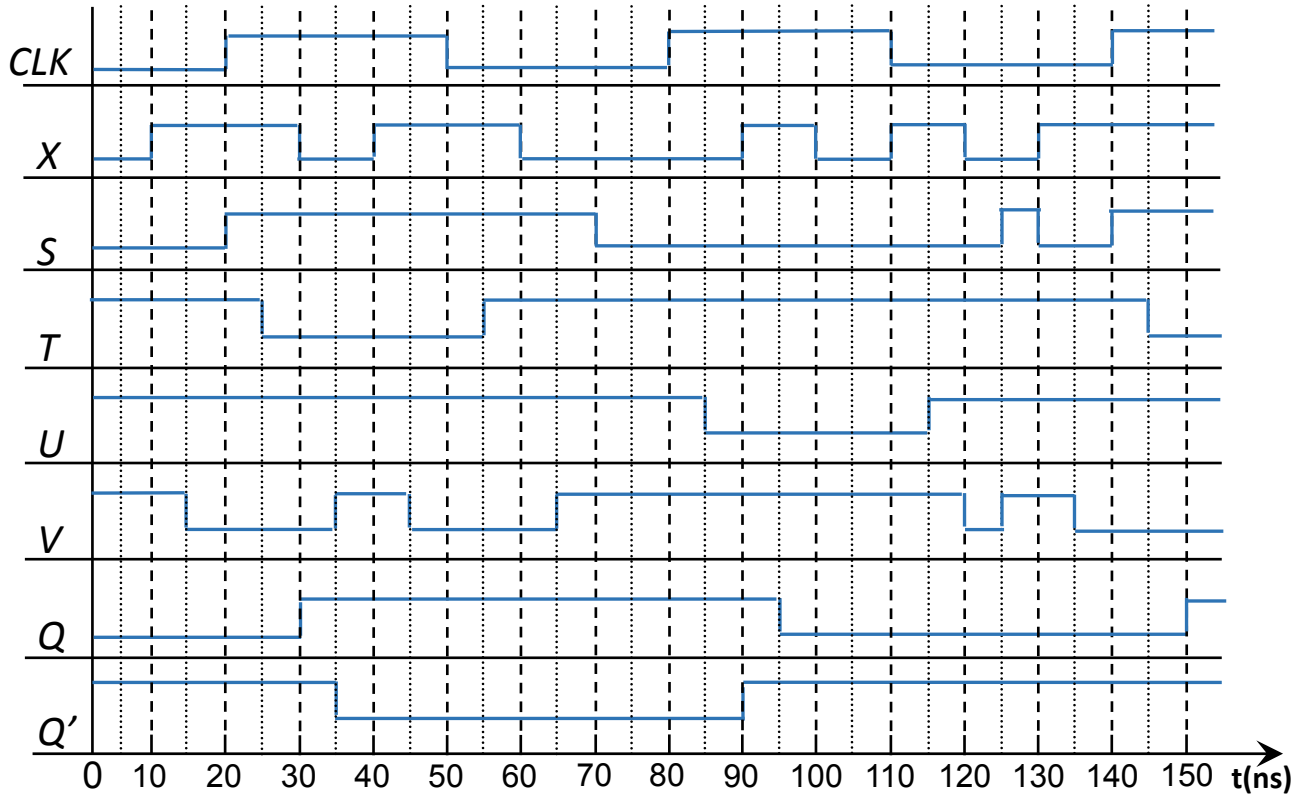
(a) (6%) Which active edge can trigger the *X* flip-flop: rising edge or falling edge?

(b) (20%) Is the *X* flip-flop edge-triggered? Explain your reasoning.

(c) (10%) Derive and minimize the next-state equation for the *X* flip-flop.

Ans:

(a)



(b)

Rising Edge

(c)

Yes.

The value of *X* at the time of the rising clock edge determines the value of *Q* and any extra changes in *X* that occur between rising clock edges have no effect on *Q*.

(d)

$Q(t+\epsilon) = X$