Logic design (2016 fall)
Quiz # 15

Name:_____ID:_____

1. (60%) Given below is income pletely specified state table.

Present State	Next State $X=0$	1	Present Output
S_0	S_1	S_0	0
S_1	S_0	S_2	0
S_2	S_3	S_4	1
S_3	S_0	S_3	0
S_4	S_0	—	0

(a) (20%) Reduce the state table to four states in two different ways by specifying proper states for the don't-care term in the state table and show the two different reduced tables.

(b) (40%) Use an implication table to determine whether your two state tables in part (a) are equivalent; if they are, prove your answer by showing equivalent states.

Ans:

(a)

Reduced table 1 (T_1)				Reduced table 2 (T_2)			
Present State	Next State $X=0$	1	Present Output	Present State	Next State $X=0$	1	Present Output
S_0	S_1	S_0	0	S_0	S_1	S_0	0
S_1	S_0	S_2	0	S_1	S_0	S_2	0
S_2	S_3	S_1	1	S_2	S_3	S_3	1
S_3	S_0	S_3	0	S_3	S_0	S_3	0

(b)

S_0:
S_1-S_1' S_0-S_0' | S_1-S_0' S_0-S_2' | | S_1-S_0' S_0-S_3'

No equivalent states

S_1:
S_0-S_1' S_2-S_0' | S_0-S_0' S_2-S_2' | | S_0-S_0' S_2-S_3'

S_2:
| | S_3-S_3' S_1-S_3' |

S_3:
S_0-S_1' S_3-S_0' | S_0-S_0' S_3-S_2' | | S_0-S_0' S_3-S_3'

S_0' S_1' S_2' S_3'
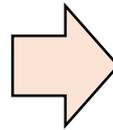
$T_1 \neq T_2$

2. (40%) Following shows the state table of a Moore sequential circuit, which has two inputs X, Y and two outputs Z_1, Z_2.

Present State	Next State $XY=00$	01	11	10	Present Output Z_1Z_2
S_0	S_0	S_3	S_0	S_3	10
S_1	S_0	S_1	S_2	S_3	01
S_2	S_1	S_1	S_2	S_2	01
S_3	S_0	S_2	S_1	S_3	11

If the sequential circuit is implemented by using primitive gates and D flip-flops based on one-hot encoding, write down and minimize output functions for Z_1, Z_2 and next-state equations for Q_0^+, Q_1^+, Q_2^+, Q_3^+, which correspond to states S_0, S_1, S_2, S_3 respectively.

Ans:

$Q_0^+ = X'Y'Q_0 + XYQ_0 + X'Y'Q_1 + X'Y'Q_3$

$Q_1^+ = X'YQ_1 + X'Y'Q_2 + X'YQ_2 + XYQ_3 = X'YQ_1 + X'Q_2 + XYQ_3$

$Q_2^+ = XYQ_1 + XYQ_2 + XY'Q_2 + X'YQ_3 = XYQ_1 + XQ_2 + X'YQ_3$

$Q_3^+ = X'YQ_0 + XY'Q_0 + XY'Q_1 + XY'Q_3$

$Z_1 = Q_0 + Q_3$

$Z_2 = Q_1 + Q_2 + Q_3$