Department of Electronics Engineering
National Chiao Tung University

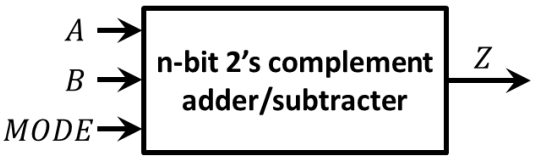
Mango Chia-Tso Chao

# Logic design (2016 fall)

## Quiz # 16

Name:_____ID:_____

1. (30%) Design an n-bit 2's complement adder/subtracter using **one** 1-bit full adder, **one** D flip-flop, and **one** exclusive-OR gate. When $MODE$ is 1, the circuit should output $A - B$, otherwise, it should output $A + B$. The definitions for inputs and outputs are shown as below.




Input signals：

$A$, $B$：n-bit serial-in 2's complement number ($A = A_n \ldots A_1 A_0$ and $B = B_n \ldots B_1 B_0$) with the LSB (least significant bit) first.

$MODE$：

0 (adder)：$Z = A + B$

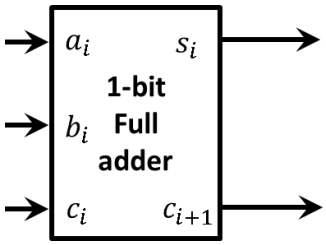
1 (subtracter)：$Z = A - B$

$Clock$：clock

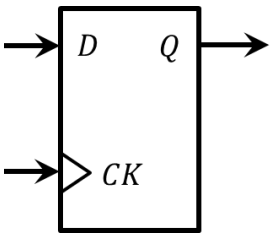
Output signals：

$Z$：n-bit serial-out 2's complement number ($Z = Z_n \ldots Z_1 Z_0$) with the LSB first.

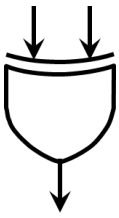
Please draw your circuit by using the following blocks.



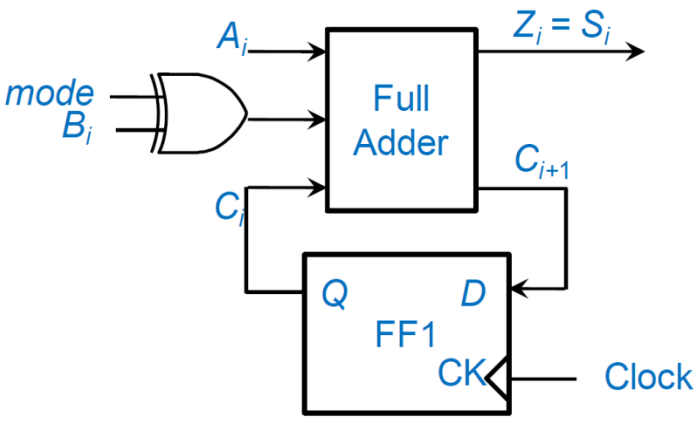

1-bit full adder




D flip-flop



exclusive-OR gate



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2. Given the transition table of a sequential circuit,
   (a) (30%) Draw a block diagram that shows how a ROM and two D flip-flops could be connected to realize the sequential circuit. Note that you must specify the size of the ROM.
   (b) (40%) Specify the contents of the PLA in the following tabular form if a PLA and two D flip-flops are used to realize the sequential circuit.

Transition table

| Present State | Next State $Q_1^+Q_2^+$ | | $Z$ |
|---|---|---|---|
| $Q_1Q_2$ | $X=0$ | $X=1$ | |
| 00 | 01 | 10 | 1 |
| 01 | 01 | 01 | 0 |
| 11 | 01 | 10 | 0 |
| 10 | 00 | 10 | 0 |

| Product term | Inputs $XQ_1Q_2$ | Outputs $ZD_1D_2$ |
|---|---|---|
| $XQ_2'$ | 1-0 | 010 |
| $XQ_1$ | 11- | 010 |
| $X'Q_1'$ | 00- | 001 |
| $X'Q_2$ | 0-1 | 001 |
| $Q_1'Q_2$ | -01 | 001 |
| $Q_1'Q_2'$ | -00 | 100 |
| | AND plane | OR plane |