Department of Electronics Engineering
National Chiao Tung University

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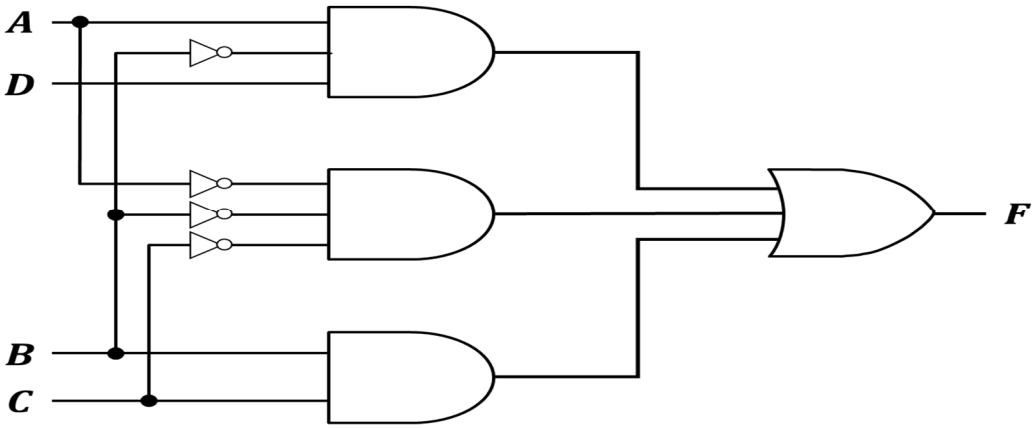
Logic design (2016 FALL)

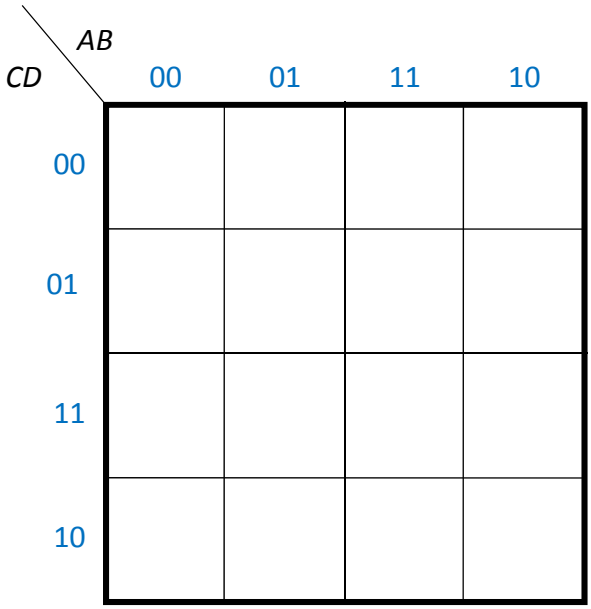
Quiz # 8

Name:_____ID:_____

1. (100%) Assuming that only one input signal can change each time, the given circuit may generate a static-1 hazard at the output F when some specific pairs of input values are supplied.
   (a)(20%) Finish the Karnaugh map for F.
   (b)(50%) Write down the terms which should be added.
   (c)(30%) Write down all possible pairs of input values which can cause a static-1 hazard at output F.



(a)



(b) F = A'B'C' + BC + AB'D

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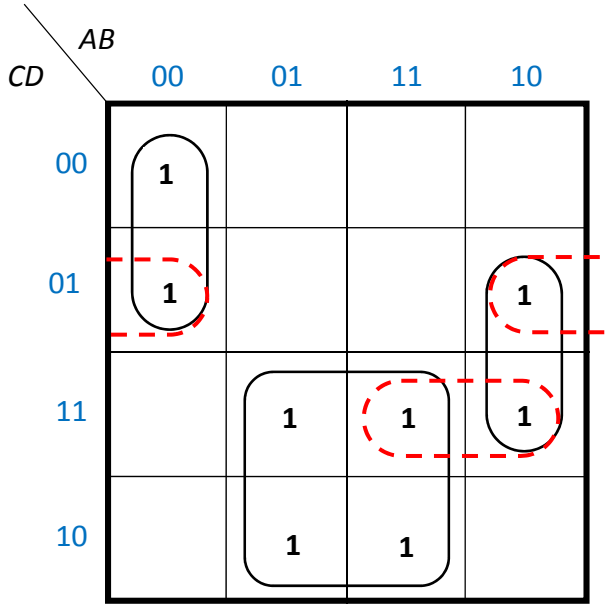
Ans:

(a)



(b) F=A'B'C' + BC + AB'D + ACD + B'C'D

(c) (A , B , C , D) = (1 , 0 , 0 , 1) -> (0 , 0 , 0 , 1)
(A , B , C , D) = (1 , 1 , 1 , 1) -> (1 , 0 , 1 , 1)