Department of Electronics Engineering
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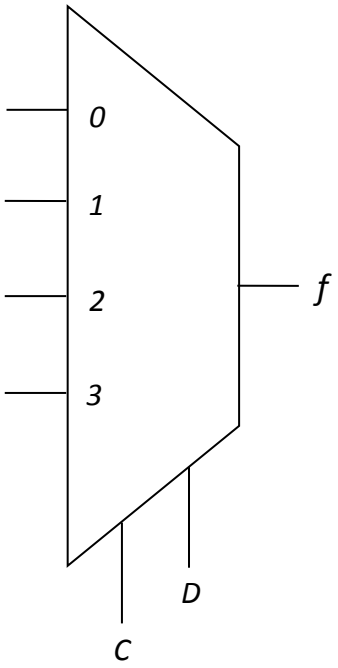
Logic design (2016 fall)

Quiz # 9

Name:_____ID:_____

1. (50%) Given $f(A,B,C,D) = C'D + AB'C' + A'BD + BC'D + ABC'D' + ABCD.$
   Implement the function f using a given 4-to-1 multiplexer with C and D as the select inputs where C is the most significant bit and D is the least significant bit. Note that complement inputs are not allowed.

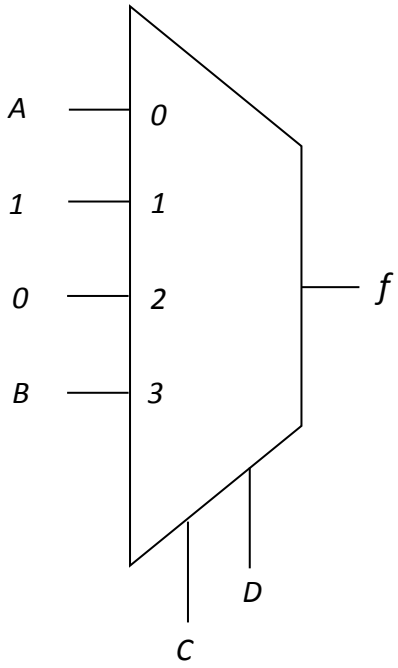


Ans:

$f(A,B,C,D) = C'D + AB'C' + A'BD + BC'D + ABC'D' + ABCD.$

$= C'D' \cdot (AB' + AB) + C'D \cdot (1 + AB' + A'B + B) + CD' \cdot (0) + CD \cdot (A'B + BC' + AB)$

$= C'D' \cdot (A) + C'D \cdot (1) + CD' \cdot (0) + CD \cdot (B)$



2. (50%) Excess-3 and 2-out-of-5 codes for decimal digits are shown in the following table.

Decimal digit	Excess-3 code	2-out-of-5 code
0	0011	00011
1	0100	00101
2	0101	00110
3	0110	01001
4	0111	01010
5	1000	01100
6	1001	10001
7	1010	10010
8	1011	10100
9	1100	11000

Specify the data stored in the following 16-word × 5-bit ROM that can realize an Excess-3 code to 2-out-of-5 code converter with four addresses inputs (*W, X, Y, Z*), representing Excess-3 code, and five data outputs (*A, B, C, D, E*), representing 2-out-of-5 code. Note that the signal *W* is the most significant bit of the address inputs and *A* is the most significant bit of data outputs.

Address Inputs				**Data Outputs**				
W	***X***	***Y***	***Z***	***A***	***B***	***C***	***D***	***E***
0	**0**	**0**	**0**					
0	**0**	**0**	**1**					
0	**0**	**1**	**0**					
0	**0**	**1**	**1**					
0	**1**	**0**	**0**					
0	**1**	**0**	**1**					
0	**1**	**1**	**0**					
0	**1**	**1**	**1**					
1	**0**	**0**	**0**					
1	**0**	**0**	**1**					
1	**0**	**1**	**0**					
1	**0**	**1**	**1**					
1	**1**	**0**	**0**					
1	**1**	**0**	**1**					
1	**1**	**1**	**0**					
1	**1**	**1**	**1**					

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Ans:

W X Y Z	*A B C D E*
0 0 0 0	X X X X X
0 0 0 1	X X X X X
0 0 1 0	X X X X X
0 0 1 1	0 0 0 1 1
0 1 0 0	0 0 1 0 1
0 1 0 1	0 0 1 1 0
0 1 1 0	0 1 0 0 1
0 1 1 1	0 1 0 1 0
1 0 0 0	0 1 1 0 0
1 0 0 1	1 0 0 0 1
1 0 1 0	1 0 0 1 0
1 0 1 1	1 0 1 0 0
1 1 0 0	1 1 0 0 0
1 1 0 1	X X X X X
1 1 1 0	X X X X X
1 1 1 1	X X X X X