Logic design (2016 spring)
Quiz # 13

Name:_____ID:_____

1. (67%) Consider the circuit shown below.
   (a) (20%) Derive the next-state equation for each FF from its input equations.
   (b) (20%) Complete the state transition table for the circuit.
   (c) (16%) Construct the state transition graph for the circuit.
       Assume $Q_1 Q_2 = 00$ is the initial state (S_0).
   (d) (5%) Does the circuit have any unused states?
   (e) (5%) Is the circuit a Mealy or Moore machine?
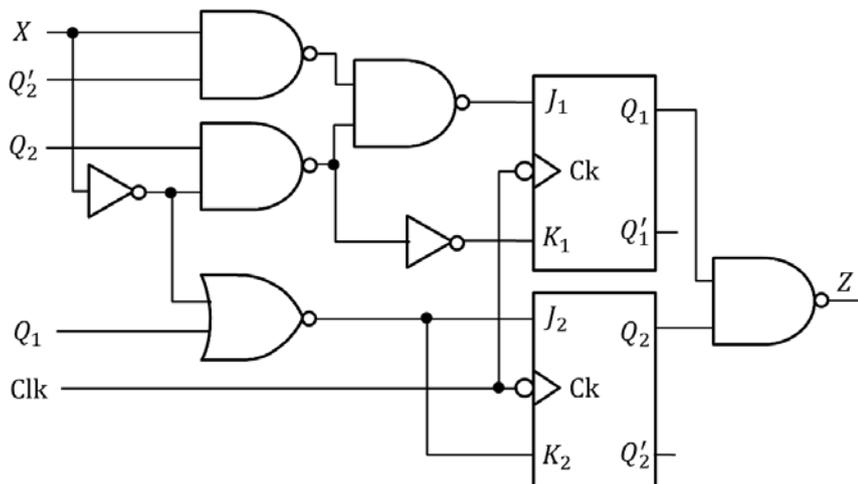
State transition table

Present State	Next State $Q_1^+ Q_2^+$		Z
$Q_1 Q_2$	$X = 0$	$X = 1$	
00	00	11	1
01	11	00	1
11	01	11	0
10	10	10	1

Ans:

$$Q_1^+ = J_1 Q_1' + K_1' Q_1$$
$$= ((XQ_2')'(X'Q_2)')'Q_1' + (((X'Q_2)')')'Q_1$$
$$= (XQ_2' + X'Q_2)Q_1' + (X + Q_2')Q_1$$
$$= XQ_1'Q_2' + X'Q_1'Q_2 + XQ_1 + Q_1 Q_2'$$
$$= XQ_2' + X'Q_1'Q_2 + XQ_1 + Q_1 Q_2'$$

$$Q_2^+ = J_2 Q_2' + K_2' Q_2$$
$$= (X' + Q_1)'Q_2' + ((X' + Q_1)')'Q_2$$
$$= XQ_1'Q_2' + X'Q_2 + Q_1 Q_2$$

$$Z = (Q_1 Q_2)' = Q_1' + Q_2'$$

The circuit is a Moore circuit. S_3 is unused.
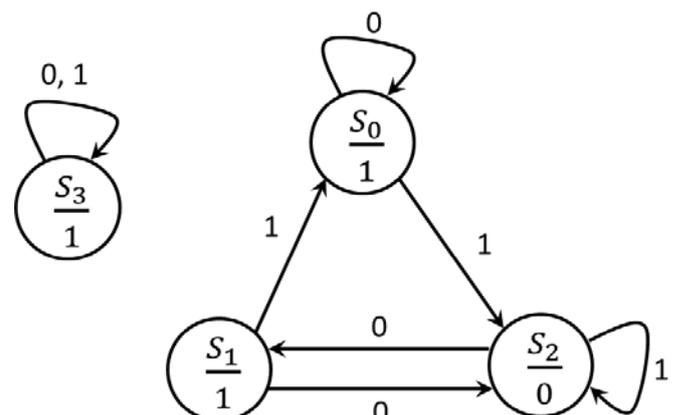
2. (34%) A sequential circuit has one input X, one output Z, and two flip-flops Q_1 and Q_2.
   The state transition table for the circuit is shown below.

Present State	Next State $(Q_1^+Q_2^+)$		Output (Z)	
(Q_1Q_2)	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	00	01	0	1
01	01	10	1	0
11	11	00	1	0
10	10	00	0	1

Assume the flip-flops are falling edge triggered, output delays of the two flip-flops are 0, the delay of any combinational circuit is 0, and $Q_1Q_2 = 00$ is the initial state.
Complete the timing chart for the circuit for the input sequence $X = 101$ and indicate any false outputs on the diagram.

Clock
X
Q_1
Q_2
Z

Clock
X
Q_1
Q_2
Z

False