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Logic design (2016 spring)

Quiz # 14

Name:_____ID:_____

A sequential circuit has one input (x) and one output (z). z can be 1 when fourth, eighth, twelfth, etc. inputs are present. And z =1 if and only if the most recent input, combined with the preceding three inputs, is not a valid excess-3 encoding of a decimal digit; otherwise, z=0. Assume excess-3 digits are received most significant bit first.

(a) (50%) Derive the state table (with description of every state) for a Mealy machine.

State	Next State		z		State Description
	x=0	x=1	x=0	x=1	
S0	S1	S2	0	0	initial state
S1	S3	S4	0	0	first bit was 0
S2	S4	S5	0	0	first bit was 1
S3	S6	S7	0	0	first 2 bits were 00
S4	S8	S8	0	0	first 2 bits were 01 or 10
S5	S9	S6	0	0	first 2 bits were 11
S6	S0	S0	1	1	first 3 bits were 000 or 111
S7	S0	S0	1	0	first 3 bits were 001
S8	S0	S0	0	0	first 3 bits were 01- or 10-
S9	S0	S0	0	1	first 3 bits were 110

(b) (50%) Derive the state table (with description of every state) for a Moore machine.

State	Next State		z	State Description
	x=0	x=1		
S0	S1	S2	0	Valid digit
S1	S3	S4	0	first bit was 0
S2	S4	S5	0	first bit was 1
S3	S6	S7	0	first 2 bits were 00
S4	S8	S8	0	first 2 bits were 01 or 10
S5	S9	S6	0	first 2 bits were 11
S6	S10	S10	0	first 3 bits were 000 or 111
S7	S10	S0	0	first 3 bits were 001
S8	S0	S0	0	first 3 bits were 01- or 10-
S9	S0	S10	0	first 3 bits were 110
S10	S1	S2	1	invalid digit