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Logic design (2016 spring)

Quiz # 15

Name:_____ID:_____

1. (60%) Two sequential circuits N_1 and N_2 have the state tables that follow.

Circuit N_1

Present State	*Next State* $X = 0$	1	*Present Output*
S_0	S_3	S_1	0
S_1	S_0	S_1	0
S_2	S_0	S_2	1
S_3	S_0	S_3	1

Circuit N_2

Present State	*Next State* $X = 0$	1	*Present Output*
A	*E*	*A*	1
B	*F*	*B*	1
C	*E*	*D*	0
D	*E*	*C*	0
E	*B*	*D*	0
F	*B*	*C*	0

(a) (40%) Without reducing the tables, determine whether circuits N_1 and N_2 are equivalent using an implication table and prove your answer by showing equivalent states.

(b) (20%) Reduce each table to a minimum number of states and show the tables.

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Ans:

(a)

	A	B	C	D	E	F
S0			~~E-S3~~ ~~D-S1~~	~~E-S3~~ ~~C-S1~~	B-S3 D-S1	B-S3 C-S1
S1			E-S0 D-S1	E-S0 C-S1	~~B-S0~~ ~~D-S1~~	~~B-S0~~ ~~C-S1~~
S2	E-S0 A-S2	F-S0 B-S2				
S3	E-S0 A-S3	F-S0 B-S3				

$A \equiv B \equiv S_2 \equiv S_3$

$C \equiv D \equiv S_1$

$E \equiv F \equiv S_0$

$N_1 \equiv N_2$

(b)

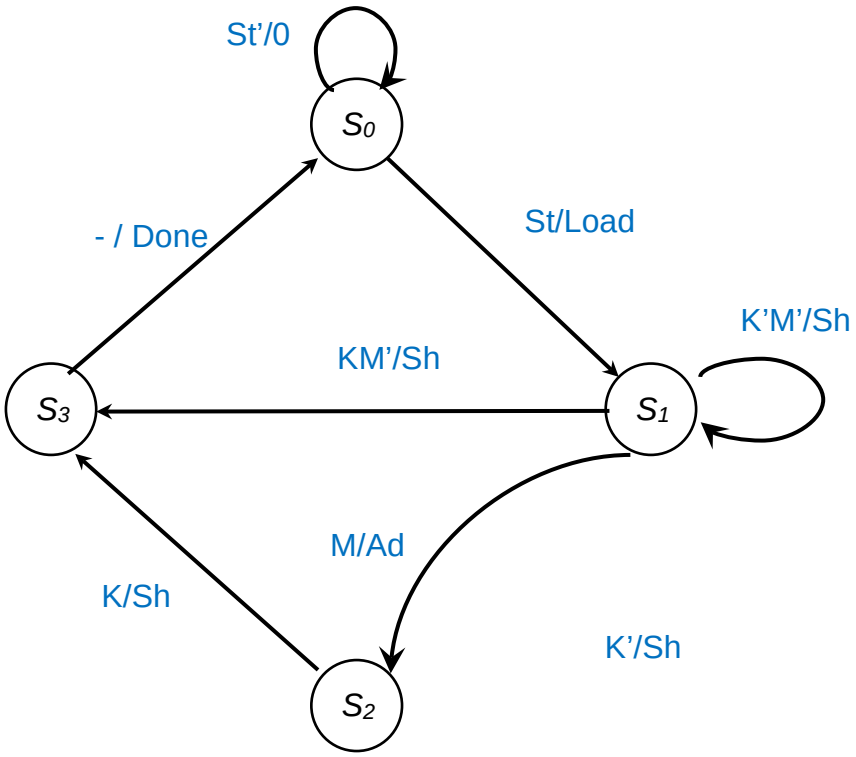
Circuit N_1

Present State	*Next State* $X = 0$	1	*Present Output*
S_0	S_2	S_1	0
S_1	S_0	S_1	0
S_2	S_0	S_2	1

Circuit N_2

Present State	*Next State* $X = 0$	1	*Present Output*
A	*E*	*A*	1
C	*E*	*C*	0
E	*A*	*C*	0

2. (40%) The state graph below represents a sequential circuit that controls a binary multiplier. The circuit has three inputs St, M, K and four outputs Load, Ad, Sh and Done.



If the given state graph is implemented using D flip-flops and primitive gates (AND, OR, NOT) only and use a one-hot assignment. Write down next-state equations for Q_0^+, Q_1^+, Q_2^+,Q_3^+ and output functions for Load, Ad, Sh and Done.

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Ans:

$Q_0^+ = Q_3 + St'Q_0$

$Q_1^+ = K'Q_2 + K'M'Q_1 + StQ_0$

$Q_2^+ = MQ_1$

$Q_3^+ = KQ_2 + KM'Q_1$

$Load = StQ_0$

$Ad = MQ_1$

$Sh = KQ_2 + K'Q_2 + K'M'Q_1 + KM'Q_1 = Q_2 + M'Q_1$

$Done = Q_3$