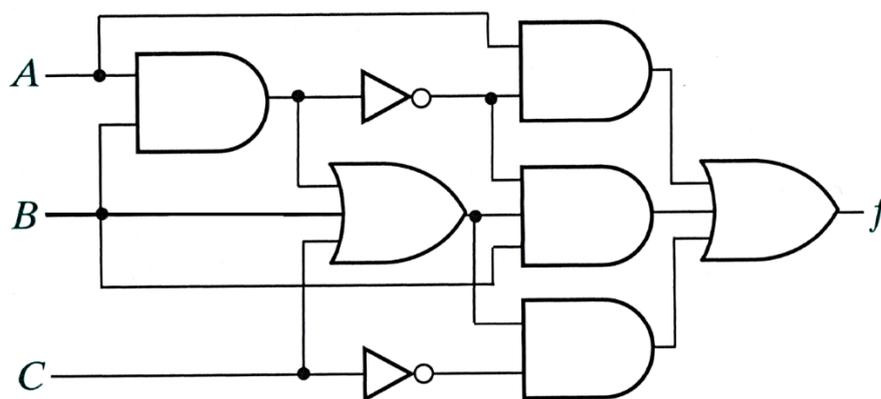


Logic design (2016 spring)

Quiz # 7

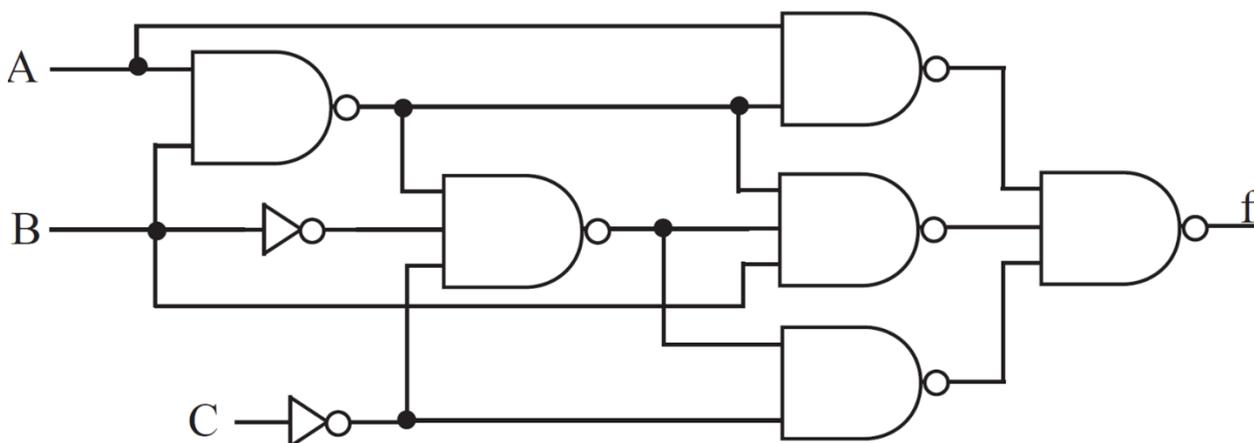
Name: _____ ID: _____

1. (40%) For the following circuit
 - (a) (10%) What is the level of the circuit?
 - (b) (30%) Use gate-equivalences to convert the circuit into a circuit containing only NAND gates and a minimum number of inverters. Note that the inputs must be in uncomplemented form.



Ans:

4



2. (60%) Two functions $f_1 = b'd + a'b' + cd$ and $f_2 = a'd' + bc + bd'$

(a) (24%) Complete the Karnaugh Maps for f_1 and f_2 .

(b) (36%) Draw a minimum two-level, multiple-output OR-AND circuit to realize f_1 and f_2 . Note that the inputs can be in complemented form.

f_1				
$cd \backslash ab$	00	01	11	10
00	1	0	0	0
01	1	0	0	1
11	1	1	1	1
10	1	0	0	0

f_2				
$cd \backslash ab$	00	01	11	10
00	1	1	1	0
01	0	0	0	0
11	0	1	1	0
10	1	1	1	0

$$f_1 = (a' + b + d)(b' + c + d')(b' + d)$$

$$f_2 = (a' + b + d)(b' + c + d')(b + d')$$

