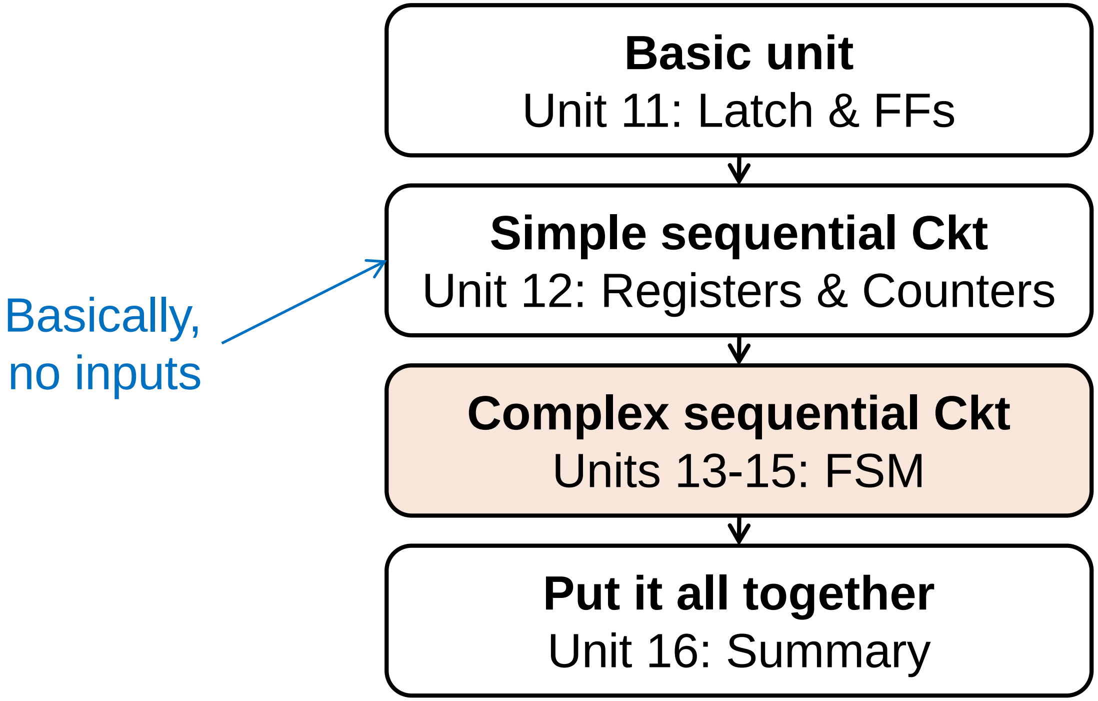
UNIT 13
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

Spring 2011

Clocked Sequential Circuits

- **Contents**
  - Analysis by signal tracing & timing charts
  - State tables and graphs
  - General models for sequential circuits
  - A sequential parity checker
- **Reading**
  - Unit 13



Basic unit
Unit 11: Latch & FFs

Simple sequential Ckt
Unit 12: Registers & Counters

Complex sequential Ckt
Units 13-15: FSM

Put it all together
Unit 16: Summary

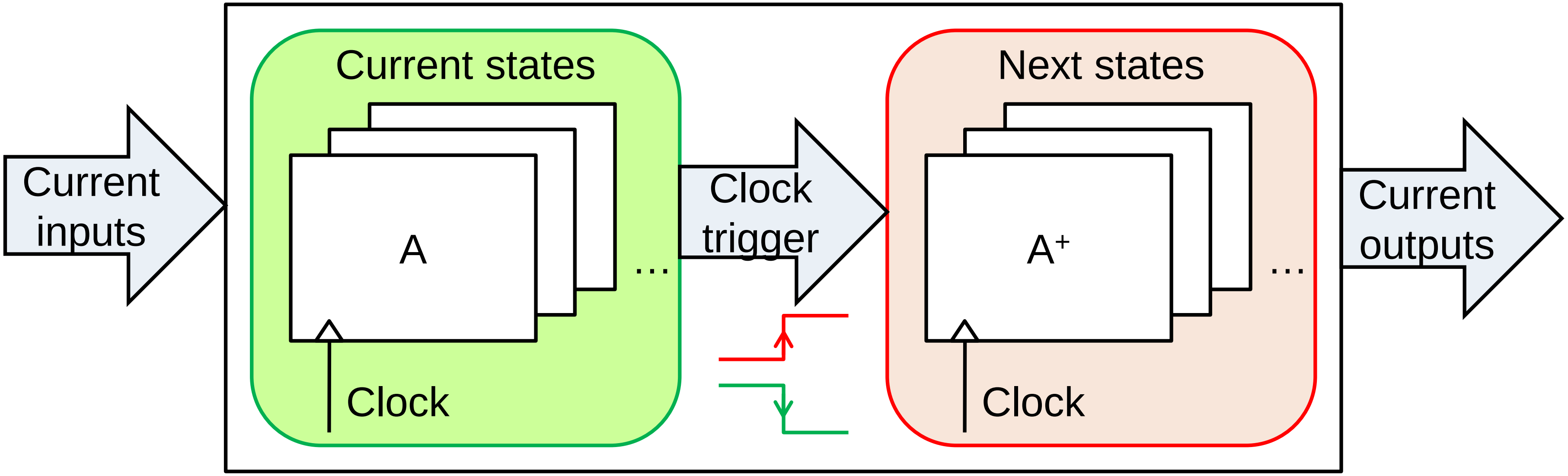
Basically, no inputs

Analysis of Clocked Sequential Circuits

- **Find the output sequence resulting from a given input one**

  ⇒ **Draw a timing chart to show inputs, clock, FF states, outputs**

  1. Assume an initial state of FFs (reset to 0)
  2. Determine the circuit outputs & FF inputs for 1st input pattern
  3. Determine the new FF states after the next active clock edge
  4. Determine the outputs for the new states
  5. Repeat 2—4 for each input pattern



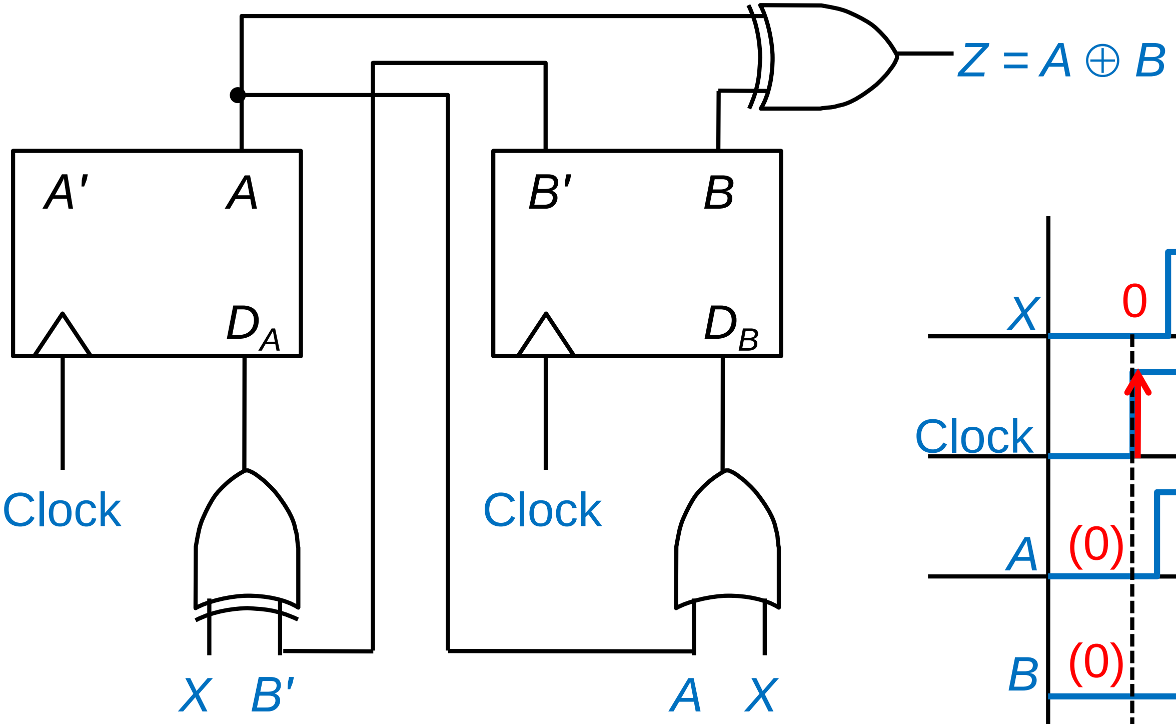
Clocked sequential ckt

Two Types of Sequential Circuits & their Timing Charts

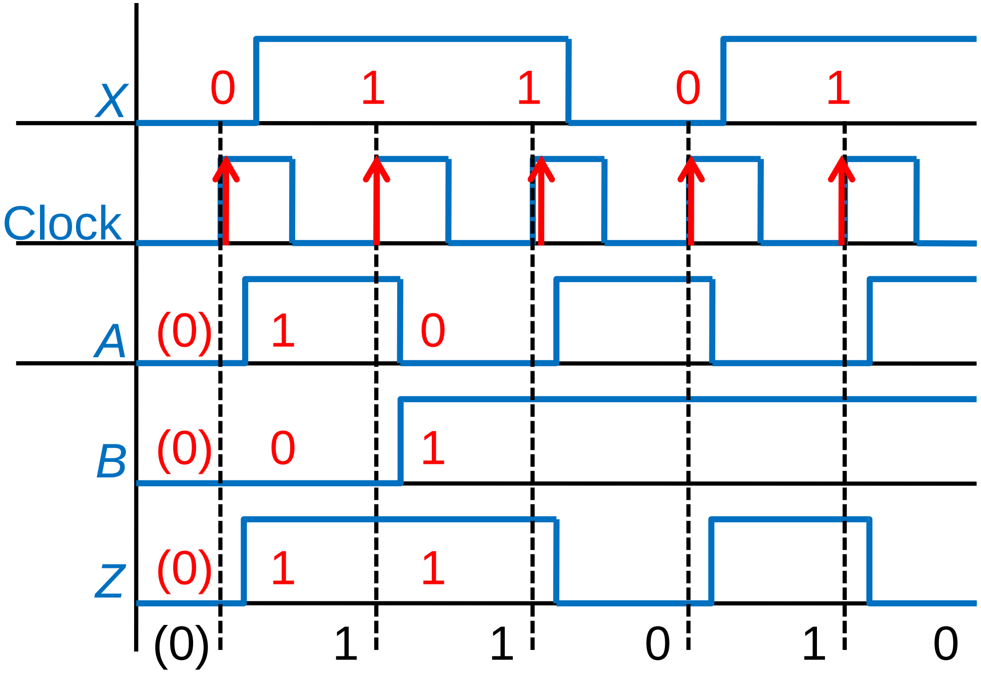
Clocked sequential ckt

Type I: Moore Machine

- **Moore machine: the output depends only on the present state**
  - The output which corresponds to a given input appears until after the active clock edge

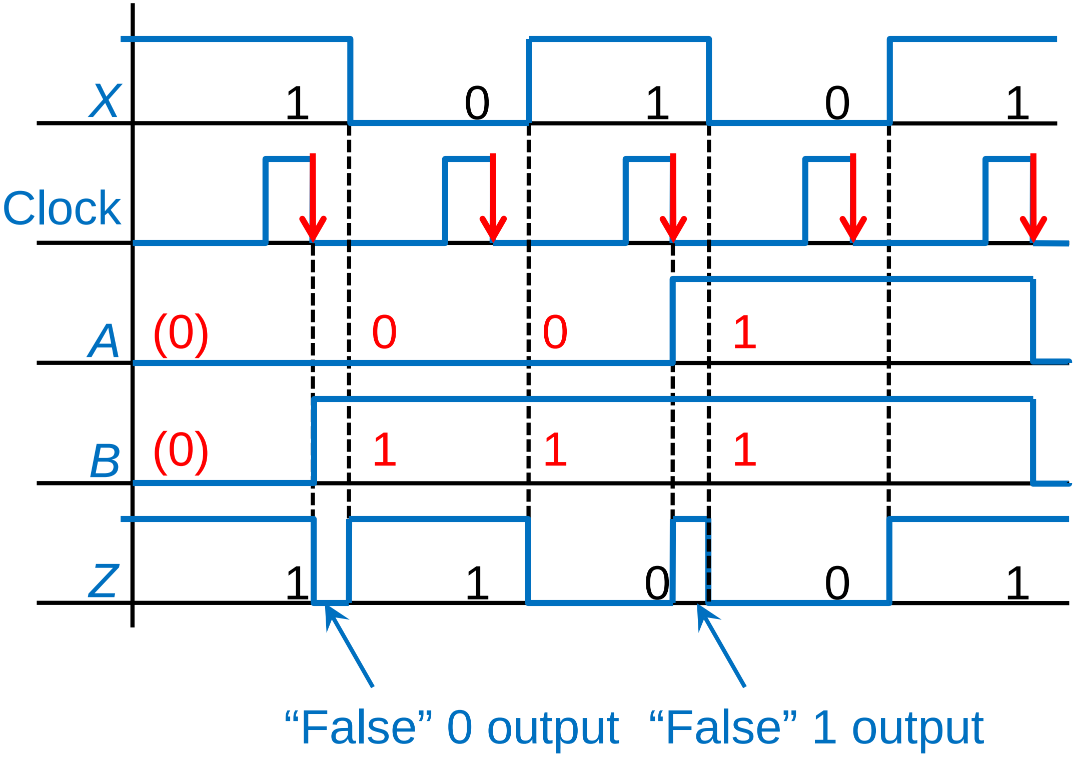


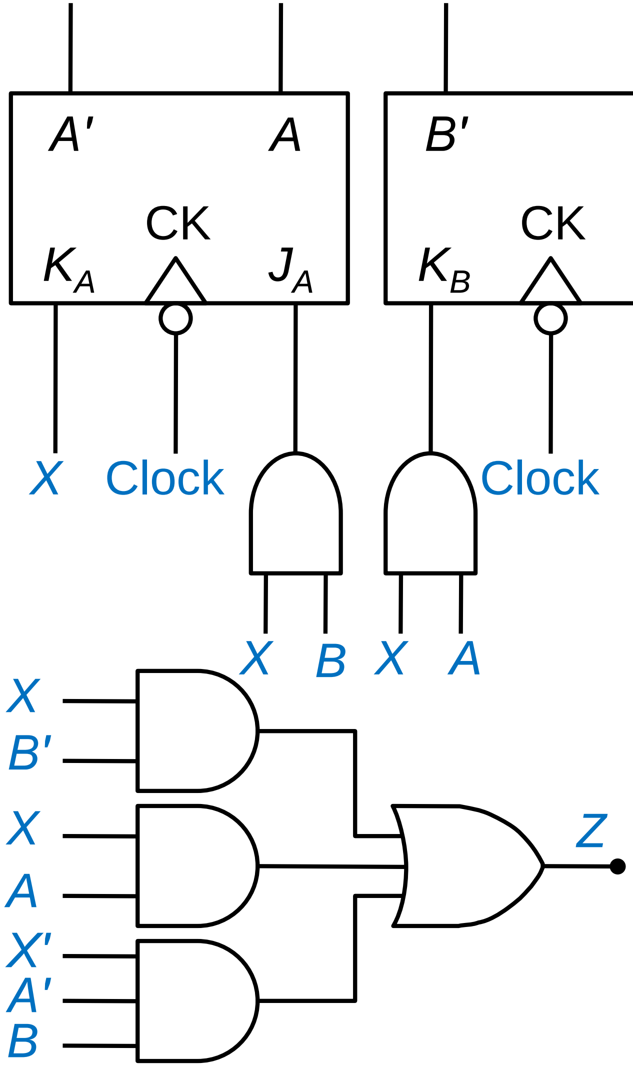
Clocked sequential ckt



Type II: Mealy Machine

- **Mealy machine: the output depends on both the present state and on the inputs**
  - False outputs may occur
    - Glitches and spikes



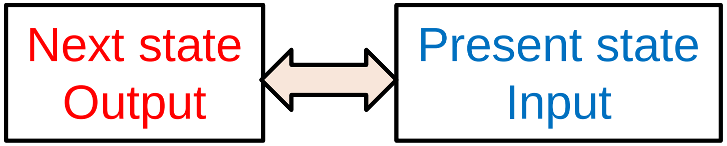


Clocked sequential ckt

State Tables and Graphs

How to Construct the State Table?

- **The state table specifies**



Next state
Output

Present state
Input

- **Procedure to construct the state table for a given circuit**
  1. Determine the flip-flop input equations and the output equations from the circuit
  2. Derive the next-state equation for each FF from its input equations
  3. Plot a next-state map for each flip-flop
  4. Combine these maps to form the state table

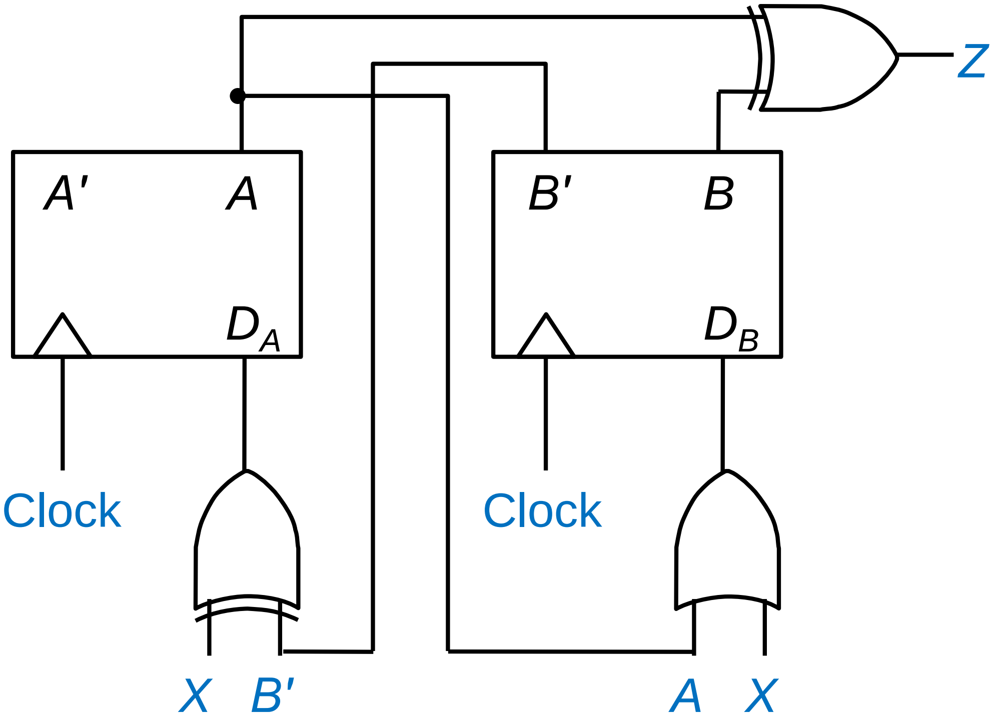
Recap Next-State Equations

Type	Q^+
D FF	$Q^+ = D$
D-CE FF	$Q^+ = D \bullet CE + Q \bullet CE'$
T FF	$Q^+ = T \oplus Q$
S-R FF	$Q^+ = S + R'Q \quad (SR = 0)$
J-K FF	$Q^+ = JQ' + K'Q$

Example: Moore Machine (1/2)

1. $D_A = X \oplus B'$
   $D_B = A + X$
   $Z = A \oplus B$

2. $A^+ = X \oplus B'$
   $B^+ = A + X$



3.

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

A^+

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

B^+

4.

	A^+B^+		
AB	$X = 0$	$X = 1$	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

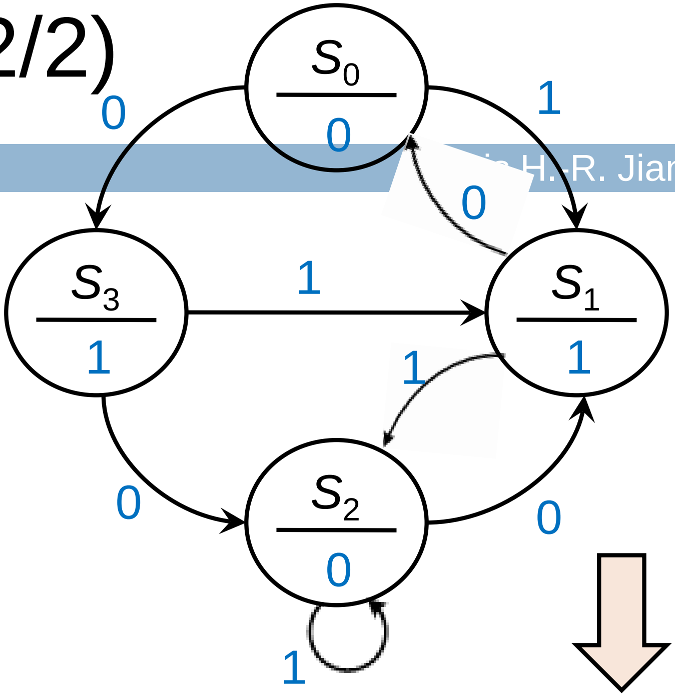
Example: Moore Machine (2/2)

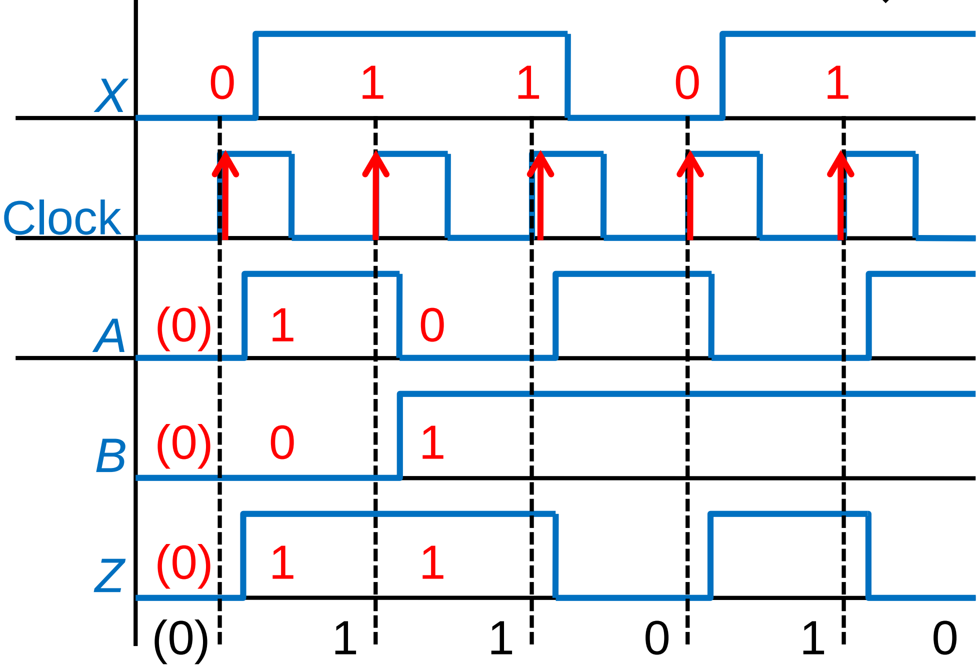
	A^+B^+		
AB	$X = 0$	$X = 1$	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

State assignment

State graph

Present state	Next state		Present output (Z)
	$X = 0$	$X = 1$	
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1





Clocked sequential ckt

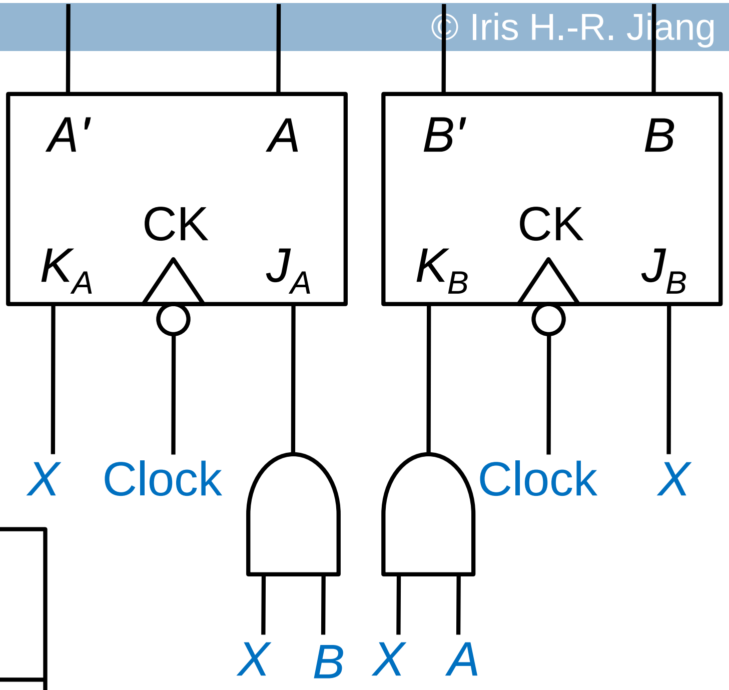
Example: Mealy Machine (1/3)

1.&2. $A^+ = J_A A' + K_A'A = XBA' + X'A$

$B^+ = J_B B' + K_B'B = XB' + (AX)'B$

$= XB' + A'B + X'B$

$Z = X'A'B + XA + XB'$



3.

AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

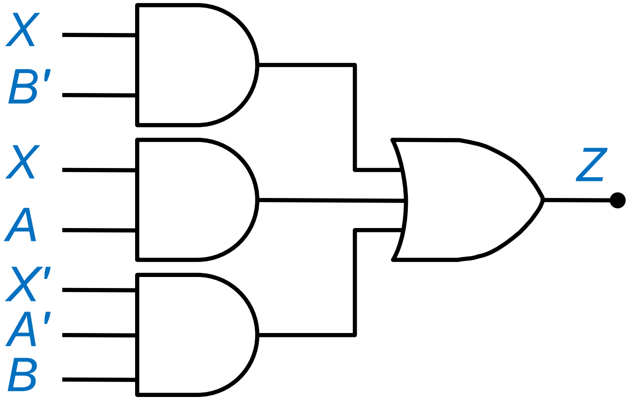
A^+

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

B^+

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Z



Example: Mealy Machine (2/3)

AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

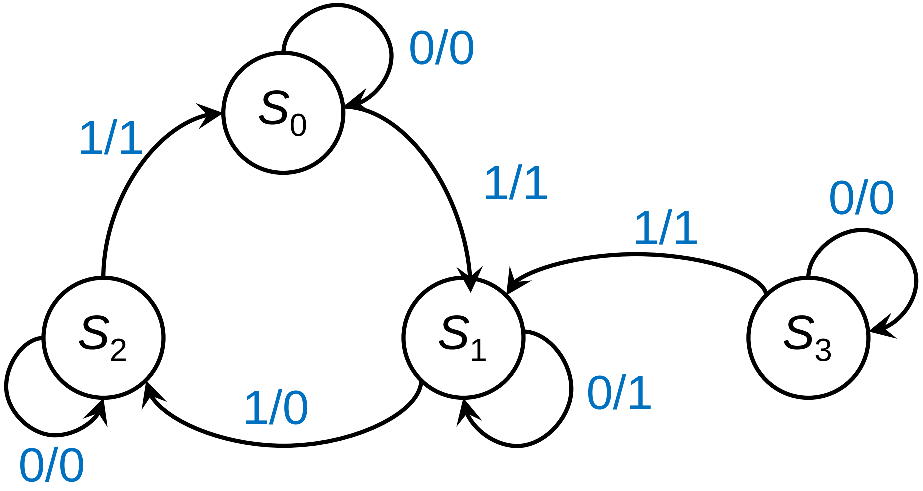
A^+

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

B^+

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Z



State graph

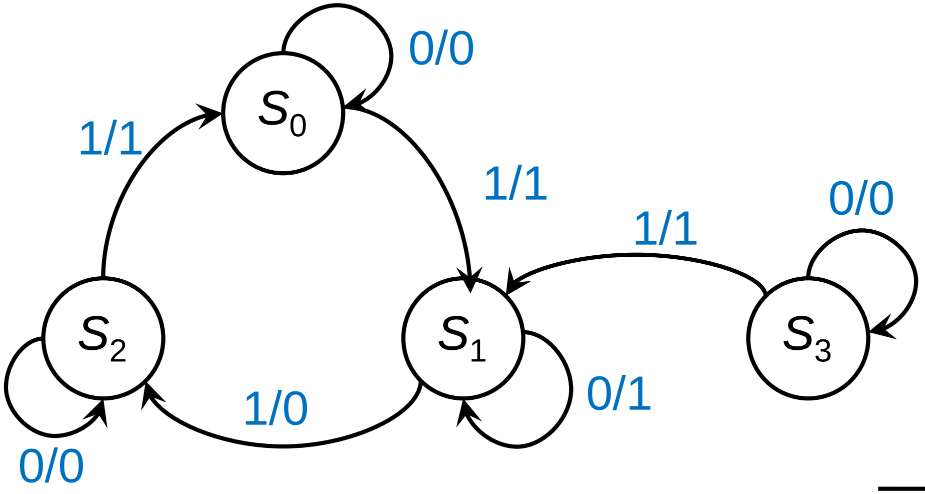
4. AB	A^+B^+ $X = 0$	 $X = 1$	Z $X = 0$	 $X = 1$
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

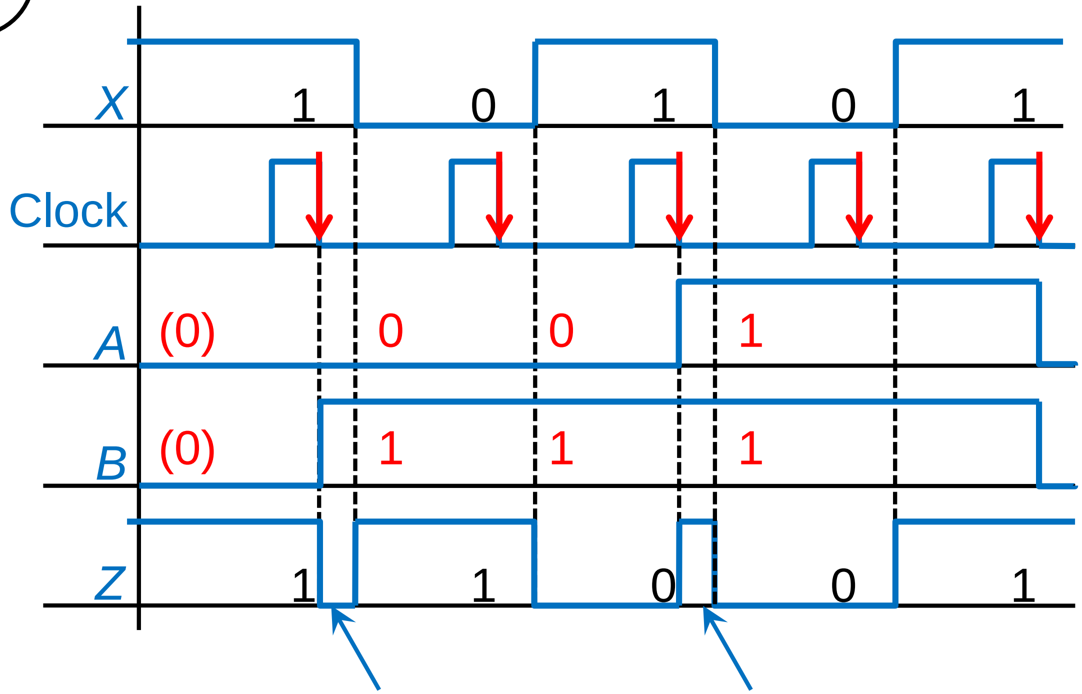
Clocked sequential ckt

State assignment

Present state	Next state $X = 0$	 $X = 1$	Present output (Z) $X = 0$	 $X = 1$
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Example: Mealy Machine (3/3)

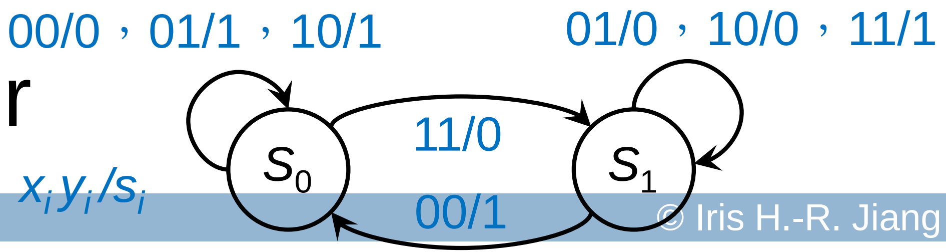




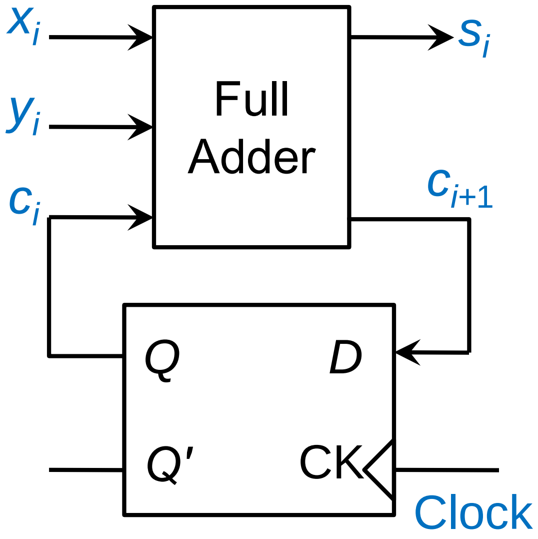
“False” 0 output “False” 1 output

Clocked sequential ckt

Example: Serial Adder

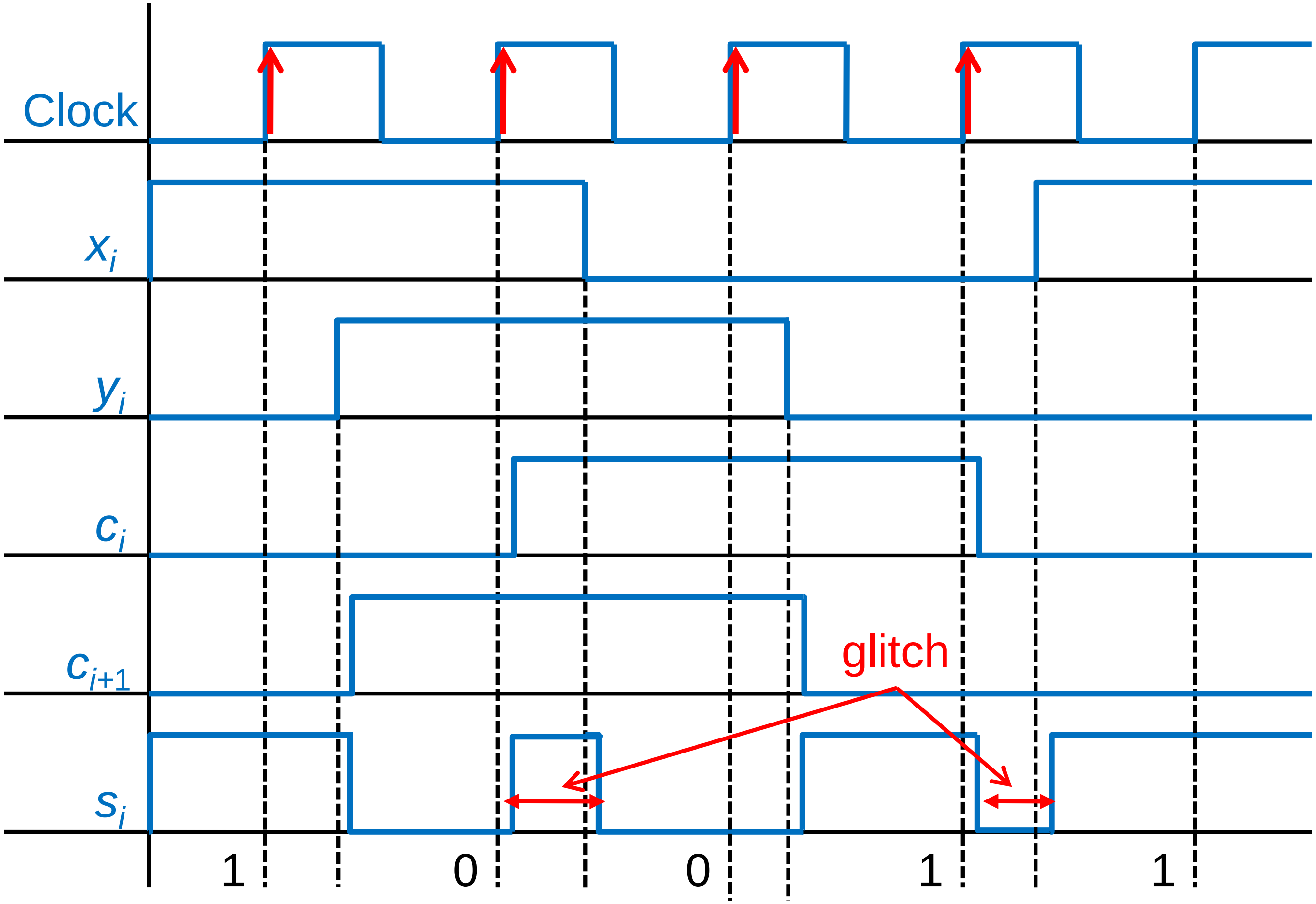


S_0: c_i=0; S_1: c_i=1



x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

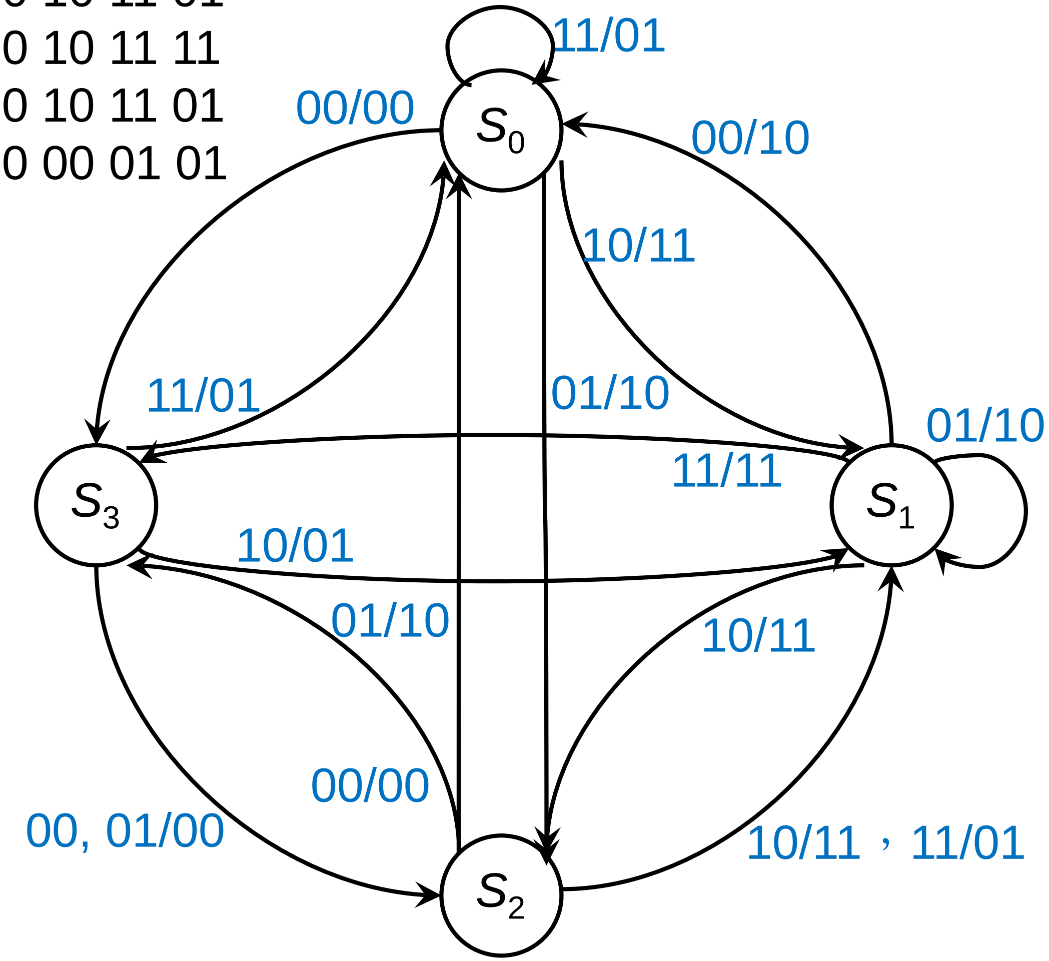
Carry_out (c_{i+1}) is latched in the DFF
The latched Carry_out will be added with the next x_i and y_i



Example: Multiple Inputs and Outputs

Present state	Next state				Present output (Z_1Z_2)			
	X_1X_2 = 00	01	10	11	X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

Q: Input X = 0 3 2 1 1 2 3 1 1 2 2
Output Z = ? (check by yourself)
State transition : $S_0S_3S_0S_1S_1$ …



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General Models

Moore vs. Mealy

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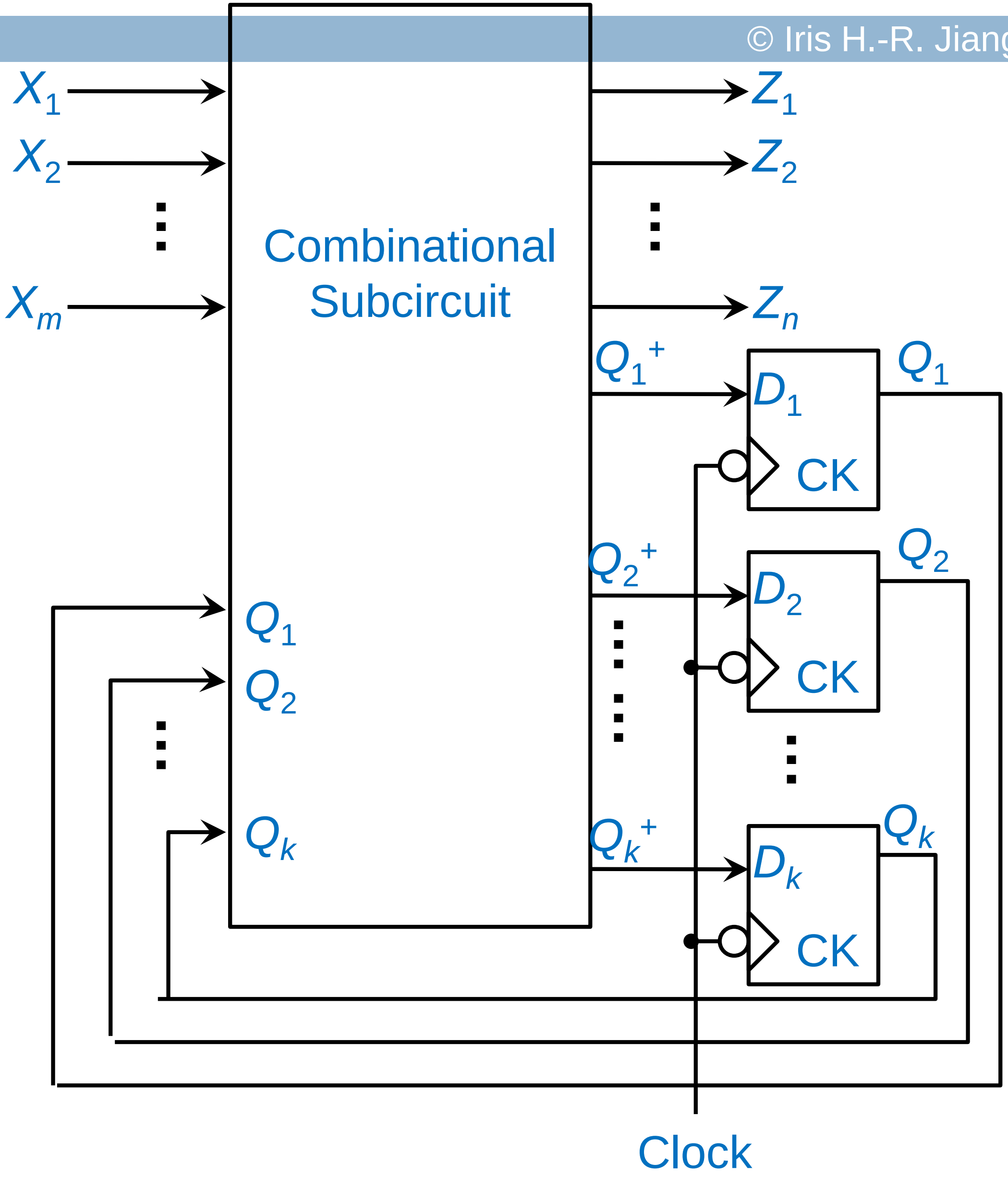
General Model for Mealy Machines

- **An output is a function of states and inputs**



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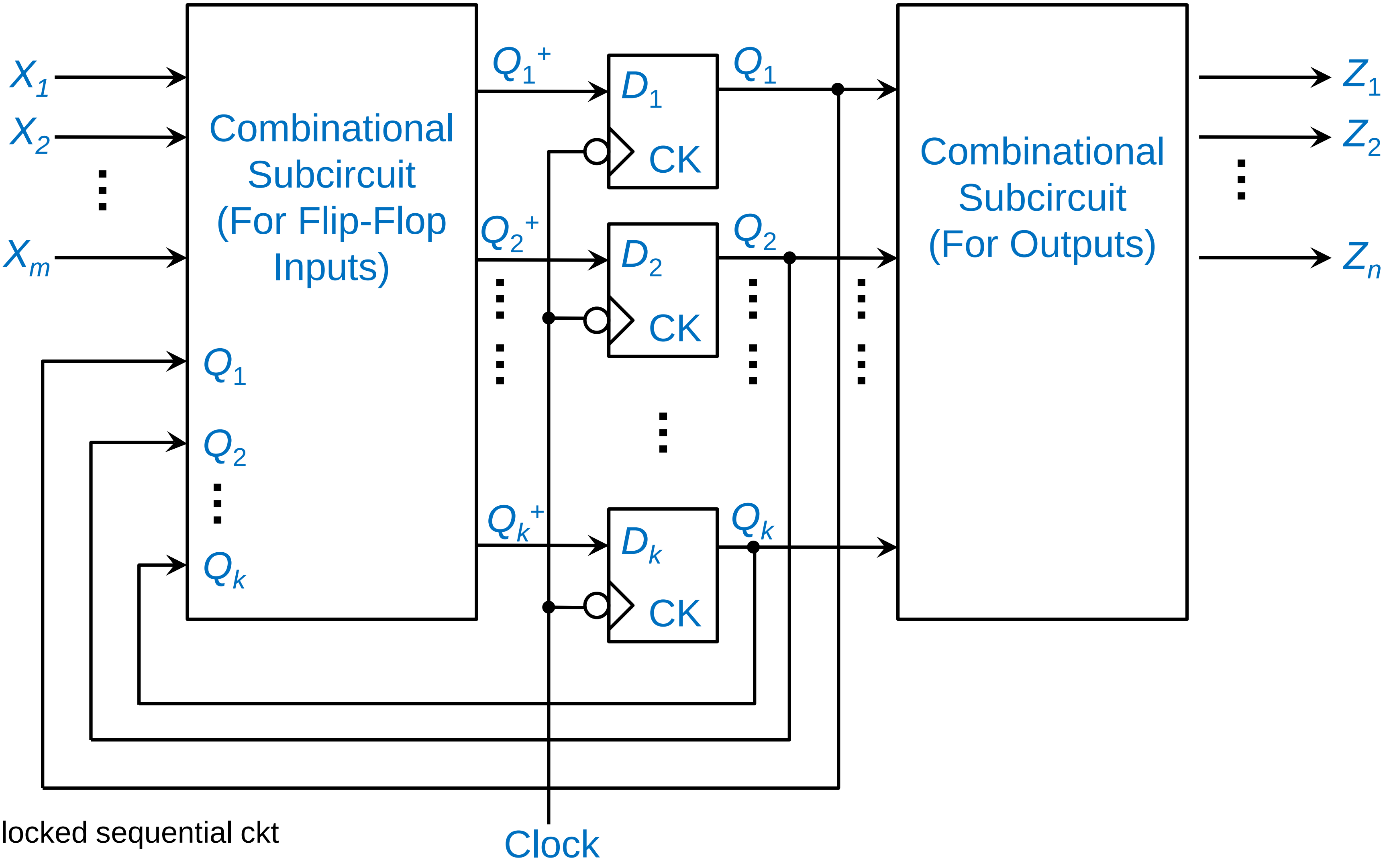
General Model for Moore Machines

- An output is a function of only states



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Case Study: A Sequential Parity Checker

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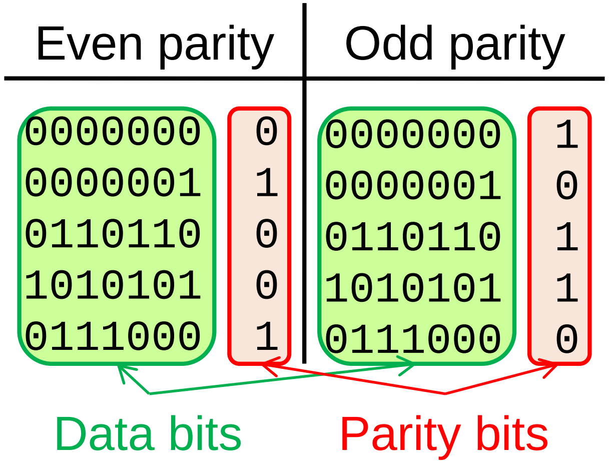
Parity Checker (1/3)

- **Error detection: add an extra bit (parity bit) when transmitting or storing binary data**
  - When the total # of 1 bits in the block (data bits + parity bit) is odd (even), we say the parity is odd (even)



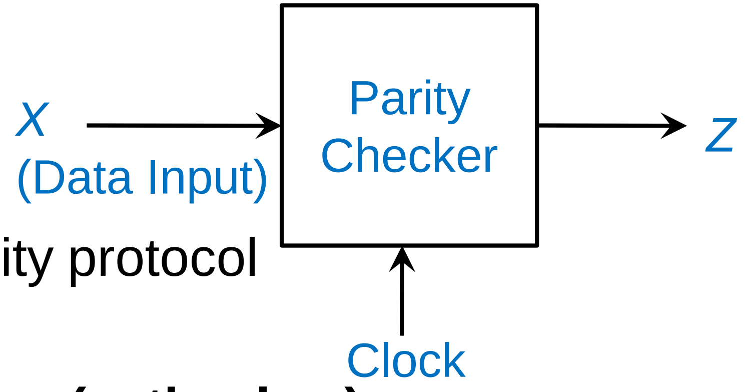
Even parity		Odd parity	
0000000	0	0000000	1
0000001	1	0000001	0
0110110	0	0110110	1
1010101	0	1010101	1
0111000	1	0111000	0

Data bits

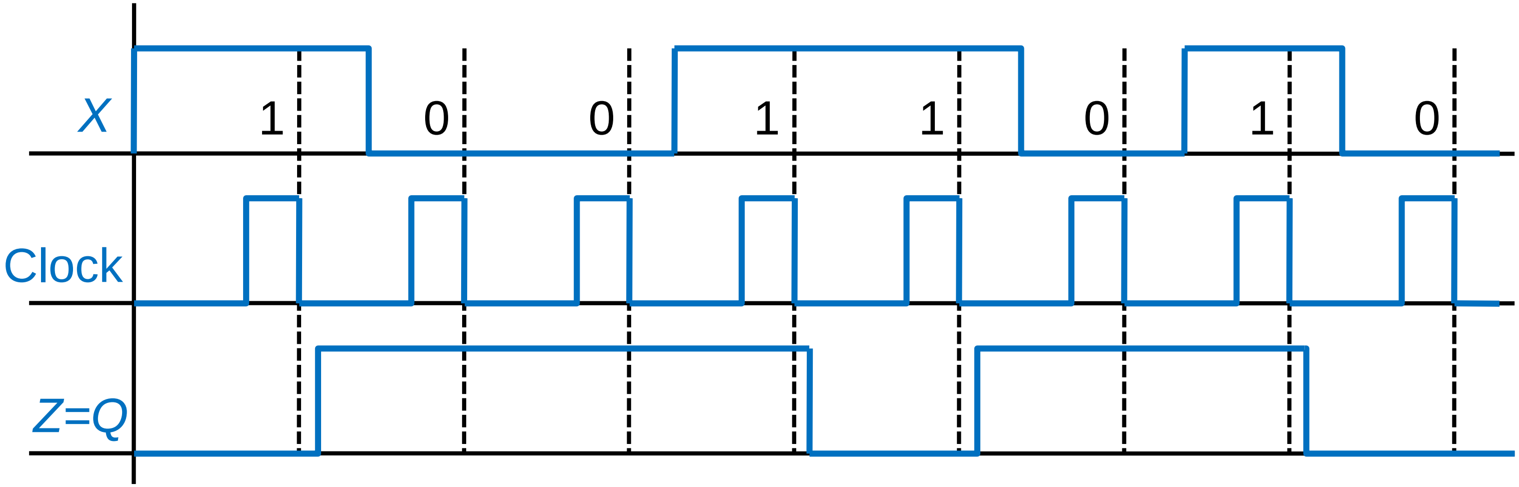
Parity bits

Parity Checker (2/3)

- **Design an odd-parity checker**
  - Z=1 if total # of 1's is odd
  - Z=0 if total # of 1's is even
    - Z=0 ⇒ an error occurs in odd-parity protocol
    - Initially, Z = 0



- **Timing chart of the odd parity checker (active-low)**



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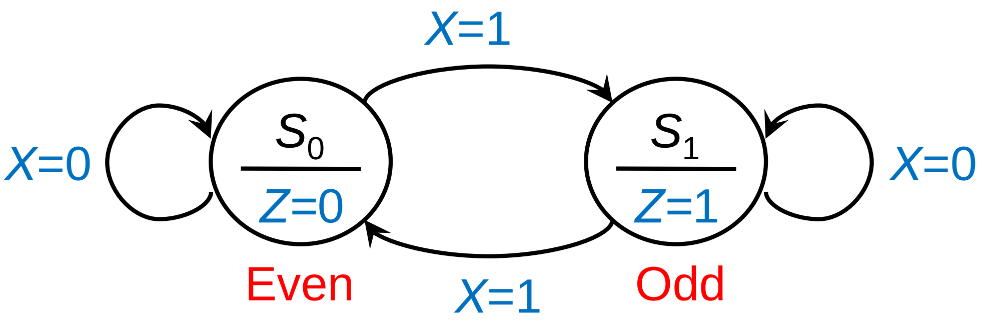
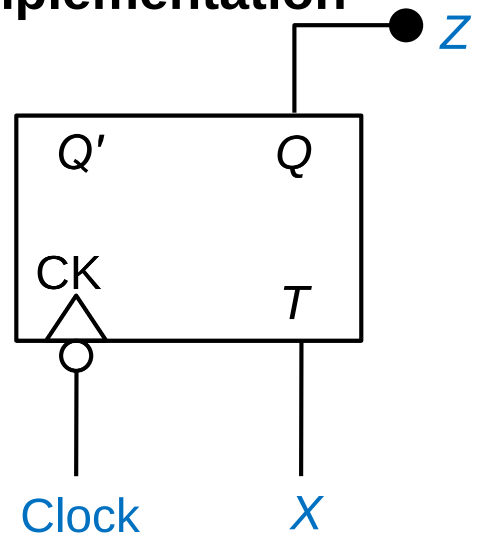
Parity Checker (3/3)

- □ **State graph**



- □ **Implementation**



- □ **State table**

Present state	Next state		Present output (Z)
	X = 0	X = 1	
S_0	S_0	S_1	0
S_1	S_1	S_0	1

Q	Q^+		Z
	X = 0	X = 1	
0	0	1	0
1	1	0	1

Clocked sequential ckt