Department of Electronics Engineering
National Chiao Tung University

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Logic design (2017 fall)

Quiz # 11

Name:_____ID:_____

1. (40%) An rising-edge-triggered AB flip-flop has two inputs A, B and one output Q, which operates as follows: When A=0 and B=0, the next clock edge resets Q to 0; when A=0 and B=1, the next clock edge leaves state unchanged; when A=1 and B=0, the next clock edge complements the state; and when A=1 and B=1, the next clock edge sets Q to 1.
   (a) (25%) Construct the state table of the AB flip-flop
   (b) (15%) Derive and minimize the next-state equation for the AB flip-flop.

Ans:

(a)

A B Q(t)	*Q(t+ϵ)*
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	1
1 0 1	0
1 1 0	1
1 1 1	1

(b)

$$Q(t+\epsilon) = AQ' + BQ$$

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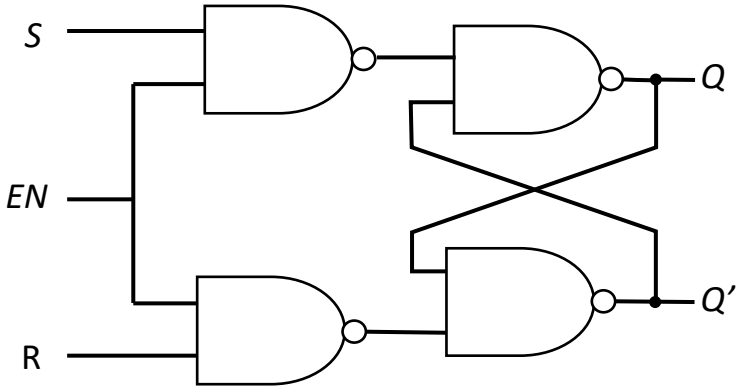
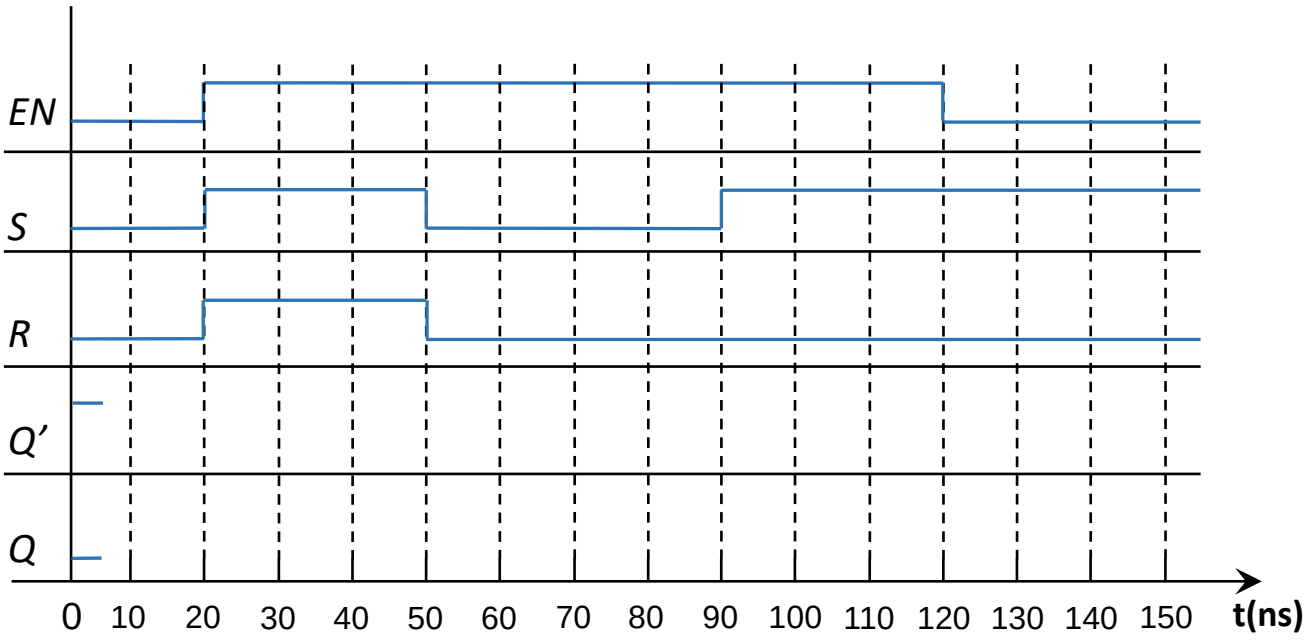
2. (60%) The function table and circuit of S-R latch with control input EN are shown below:

EN	S	R	Operation
0	X	X	No state change
1	0	0	No state change
1	0	1	Reset Q to 0
1	1	0	Set Q to 1
1	1	1	Indeterminate



Complete the following timing diagram, assuming initial Q=0, Q'=1 and each NAND gate has the same propagation delay 10ns.



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Ans: