Department of Electronics Engineering
National Chiao Tung University

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Logic design (2017 fall)

Quiz # 12

Name:_____ID:_____

The counter to be designed is a counter with 3 flip-flops denoted as a, b and c. After each clock cycle, the binary value of abc (a as the most significant bit and c as the least significant bit) will be increased by 2 except the following two conditions: (1) when abc= 110, $a^+b^+c^+$ will be 001 and (2) when abc= 111, $a^+b^+c^+$ will be 000. Please complete the following truth table and k-map of both D-FF and T-FF, and design the counter by using T-FF.

(a) (5%) Fill the next state table for this counter?

abc	$a^+b^+c^+$
000	
001	
010	
011	
100	
101	
110	
111	

(b) (15%) If D flip-flops are used, what are the input map of each flip-flop?

D_a

bc \ a	0	1
00		
01		
11		
10		

D_b

bc \ a	0	1
00		
01		
11		
10		

D_c

bc \ a	0	1
00		
01		
11		
10		

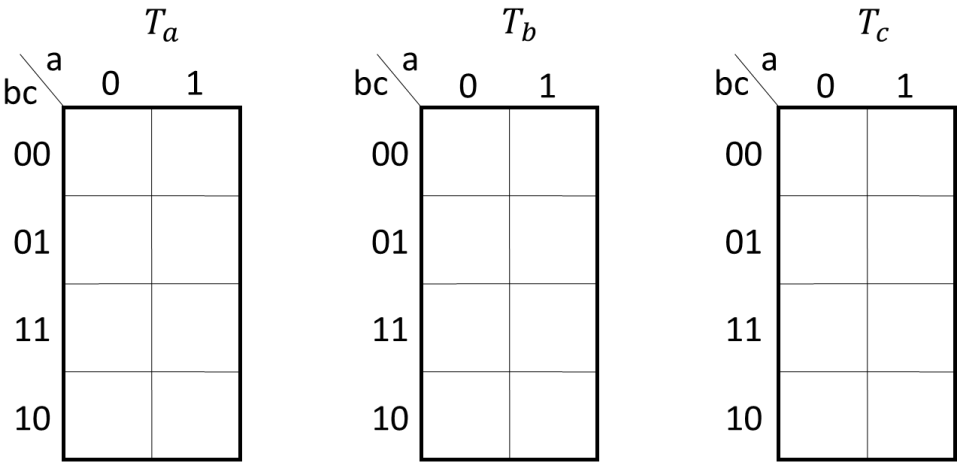
(c) (10%) Simplify the Boolean expression of each flip-flop input (in minimum sum-of-product).

D_a =

D_b =

D_c =

(d) (30%) If T flip-flops are used, what are the input map of each flip-flop?



(e) (40%) Design the counter in Figure_1. Note that you can only use 2-input AND gate, 2-input OR gate and inverter to implement the counter.

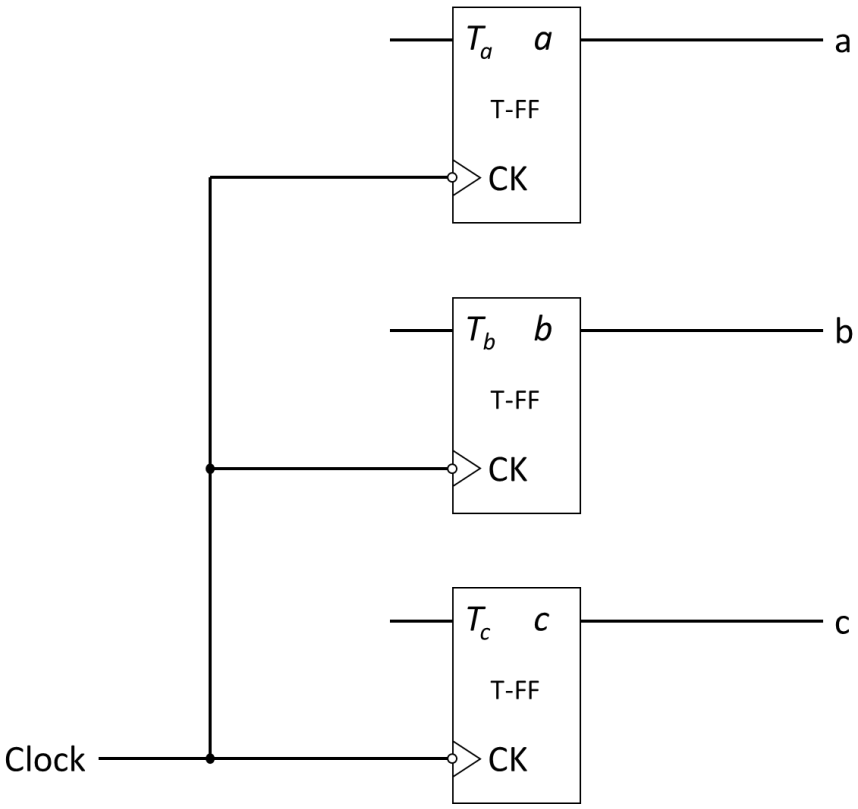


Figure_1

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(a) (20%) Use D flip-flops.

abc	$a^+b^+c^+$
000	010
001	011
010	100
011	101
100	110
101	111
110	001
111	000

a^+

bc \ a	0	1
00	0	1
01	0	1
11	1	0
10	1	0

b^+

bc \ a	0	1
00	1	1
01	1	1
11	0	0
10	0	0

c^+

bc \ a	0	1
00	0	0
01	1	1
11	1	0
10	0	1

(b) (10%) Boolean equation

$A^+ = ab' + a'b$

$B^+ = b'$

$C^+ = b'c + a'c + abc'$

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(c) (30%) Use T flip-flops.

abc	$a^+b^+c^+$	$T_a\ T_b\ T_c$
000	010	010
001	011	010
010	100	110
011	101	110
100	110	010
101	111	010
110	001	111
111	000	111

T_a

bc \ a	0	1
00	0	0
01	0	0
11	1	1
10	1	1

T_b

bc \ a	0	1
00	1	1
01	1	1
11	1	1
10	1	1

T_c

bc \ a	0	1
00	0	0
01	0	0
11	0	1
10	0	1

(d) (40%) Design the counter in figure_1. Note that you can only use 2 input ***AND***, ***OR*** and ***INV*** gate to finish the combinational part.