Department of Electronics Engineering
National Chiao Tung University

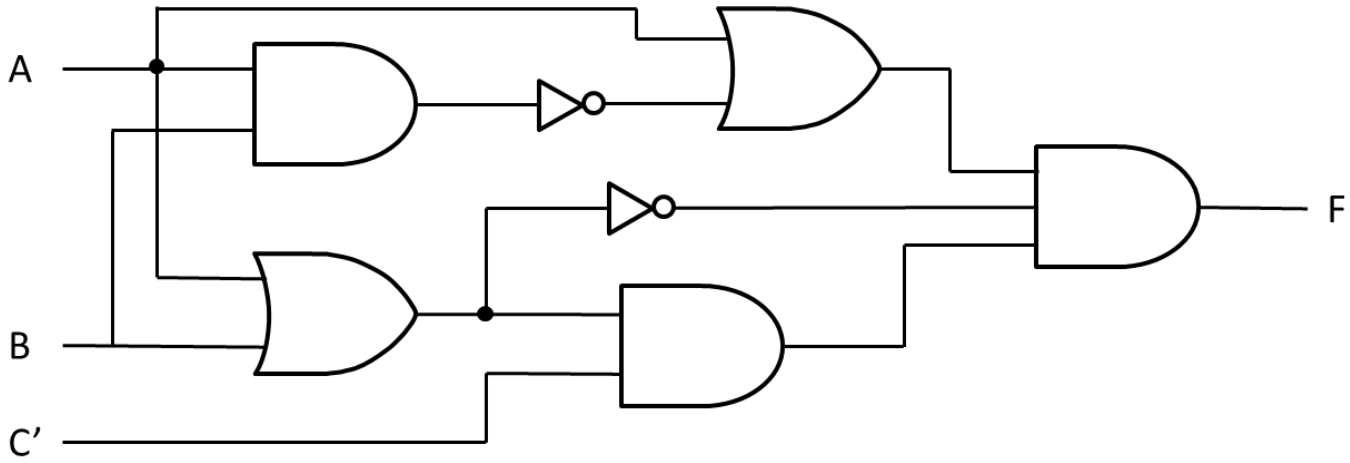
Mango Chia-Tso Chao

Logic design (2017 fall)

Quiz # 7

Name:_____ID:_____

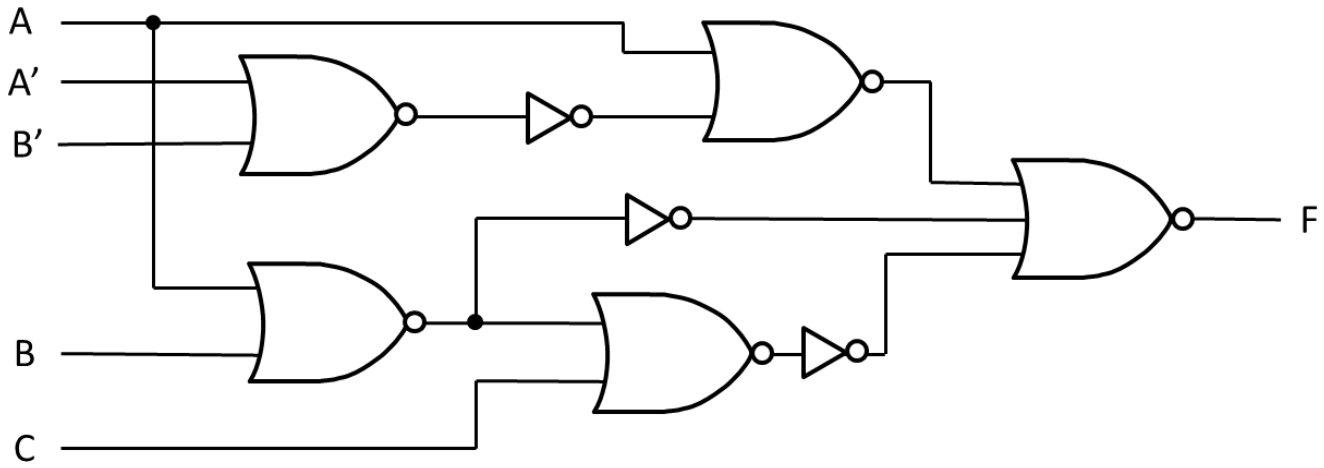
1. (50%) For the following circuit
   (a) (10%) What is the level of the circuit?
   (b) (40%) Use gate-equivalences to convert the circuit into a circuit containing only NOR gates and **least** NOT gates. Note that the inputs can be in complemented form. Also, inverters not at inputs are counted as one level but inverters at inputs are not counted.



Ans:

(a) 4

(b)



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2. (50%) Given the Karnaugh Maps for f_1 and f_2.

f_1

cd \ ab	00	01	11	10
00	0	1	1	1
01	1	1	0	X
11	0	X	0	0
10	0	X	0	X

f_2

cd \ ab	00	01	11	10
00	X	1	X	1
01	0	0	1	0
11	0	0	X	0
10	1	X	1	0

Draw a minimum two-level, multiple-output AND-OR circuit to realize f_1 and f_2 (using minimum number of gates and minimum number of gate inputs). Note that the inputs can be in complemented form.

$f_1 = a'b + a'c'd + ac'd' \quad or \quad a'b + b'c'd + ac'd'$
$f_2 = a'd' + ab + ac'd'$