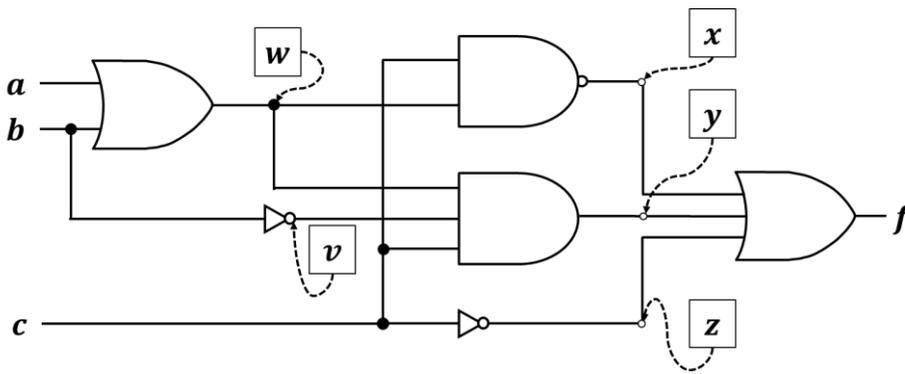Logic design (2016 FALL)
Quiz # 8

Name:_____ID:_____

1. (100%) Draw the signal waveforms of *v, w, x, y, z* and output *f* for the following circuit in figure_1. The signal waveforms of inputs *a, b* and *c* are provided in the following timing diagram already. The delay of each gates are showed in the delay table, table_1.

figure_1

GATE	delay(ns)
2_input_NAND	2
2_input_OR	3
3_input_AND	4
3_input_OR	4
INV	1

table_1