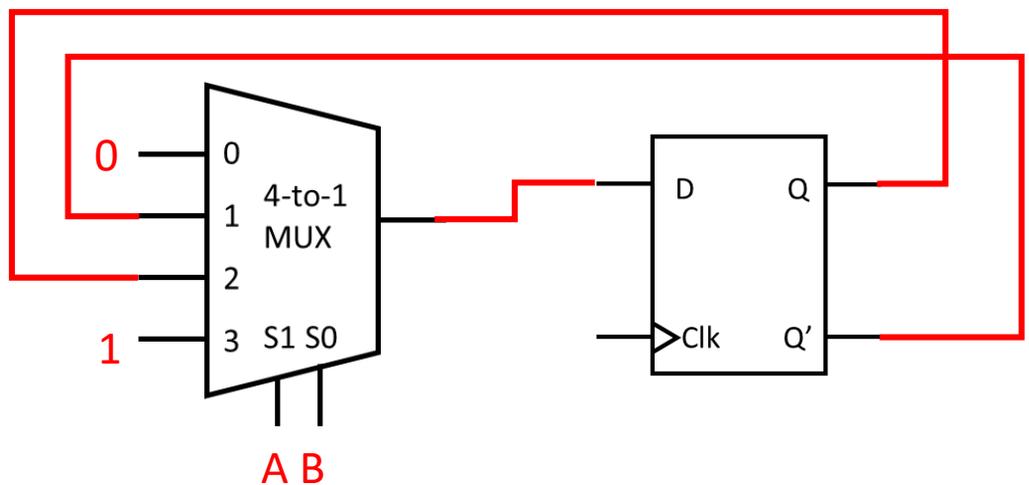


Logic design (2018 fall)
Quiz # 11

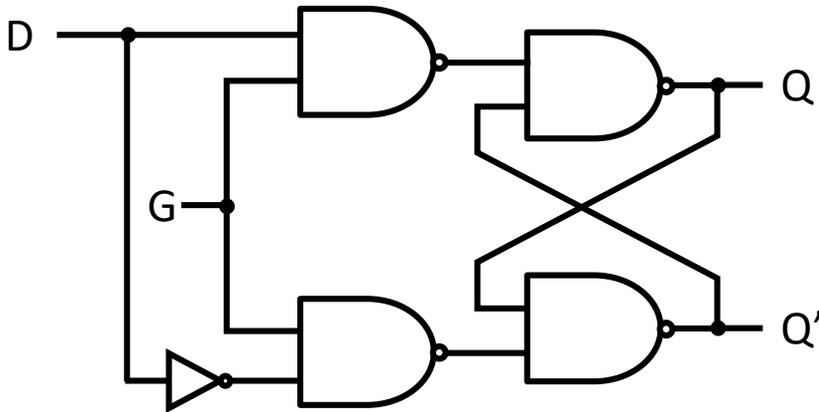
Name: _____ ID: _____

1. (50%) An rising-edge-triggered AB flip-flop has two inputs A, B and one output Q, which operates as follows: When A=0 and B=0, the next clock edge resets Q to 0; when A=1 and B=0, the next clock edge leaves state unchanged; when A=0 and B=1, the next clock edge complements the state; and when A=1 and B=1, the next clock edge sets Q to 1.
- (a) (30%)Construct the state table of the AB flip-flop.
(b) (20%)Convert a D flip-flop to the AB flip-flop by adding a 4-to-1 multiplexer.

A	B	Q(t)	Q(t+ ϵ)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



2. (50%) The circuit of gated D latch is shown below:



Complete the following timing diagram, assuming initial $Q=1$, $Q'=0$ and each NAND gate and inverter has the same propagation delay 1ns.

