

Logic design (2018 fall)

Quiz # 7

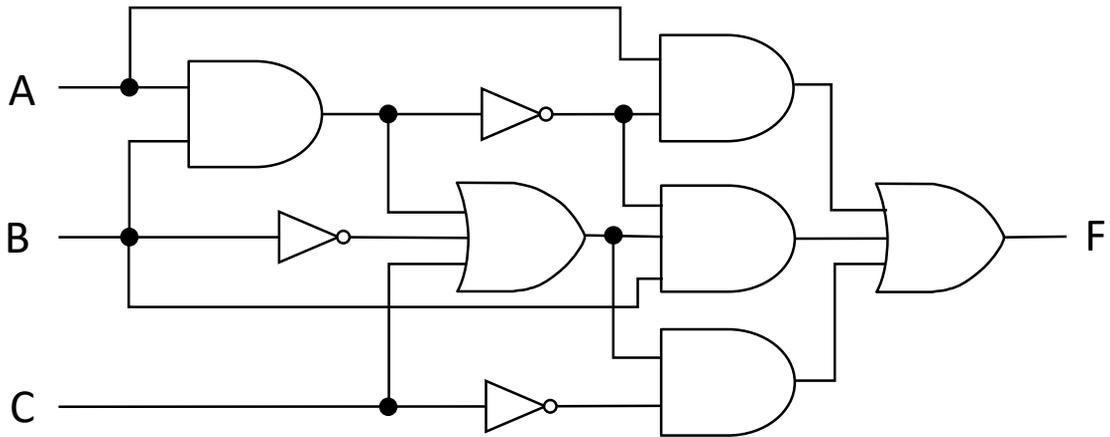
Name: _____ ID: _____

1. (50%) For the following circuit

(a) (10%) What is the level of the circuit?

(b) (40%) Use gate-equivalences to convert the circuit into a circuit containing only NAND gates and least NOT gates.

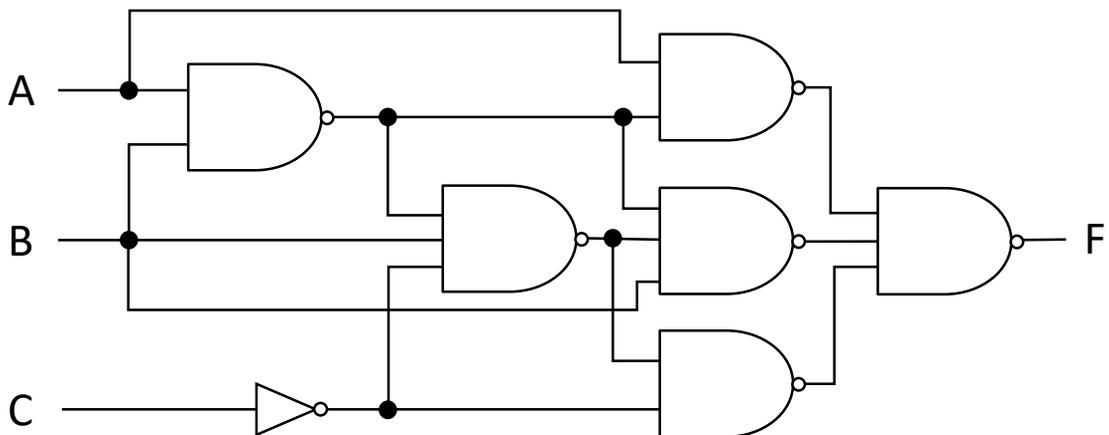
Note that the inputs must be in uncomplemented form. Inverters are counted as one level.



ANS:

(a) 4

(b)



2. (50%) Given the Karnaugh Maps for f1 and f2

ab \ cd	00	01	11	10
00	0	1	0	0
01	1	1	0	0
11	1	1	0	0
10	0	1	1	1

ab \ cd	00	01	11	10
00	0	0	0	1
01	1	1	0	1
11	1	1	0	0
10	0	0	1	1

Draw a minimum two-level, multiple-output AND-OR circuit to realize f1 and f2 (using minimum number of gates and minimum number of gate inputs). Note that the inputs can be in complemented form.

ANS:

$$f1 = a'b + a'd + acd'$$

$$f2 = a'd + acd' + ab'c'$$

