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Logic design (Fall 2021)

Quiz # 11

Name:_____ID:_____

1. (40%) An rising-edge-triggered AB flip-flop has two inputs A, B and one output Q, which operates as follows: When A=0 and B=0, the next clock edge resets Q to 0; when A=1 and B=0, the next clock edge leaves state unchanged; when A=0 and B=1, the next clock edge complements the state; and when A=1 and B=1, the next clock edge sets Q to 1.

   (40%) An rising-edge-triggered AB flip-flop has two inputs A, B and one output Q, which operates as follows: When A=0 and B=0, the next clock edge resets Q to 0; when A=0 and B=1, the next clock edge leaves state unchanged; when A=1 and B=0, the next clock edge complements the state; and when A=1 and B=1, the next clock edge sets Q to 1.

   (a) (24%) Construct the state table of the AB flip-flop.
   (b) (16%) Derive and minimize the next-state equation for the AB flip-flop

   Ans:

   (a)

A	B	Q(t)	Q(t+ϵ)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

   (b) Q(t+ϵ) = BQ' + AQ

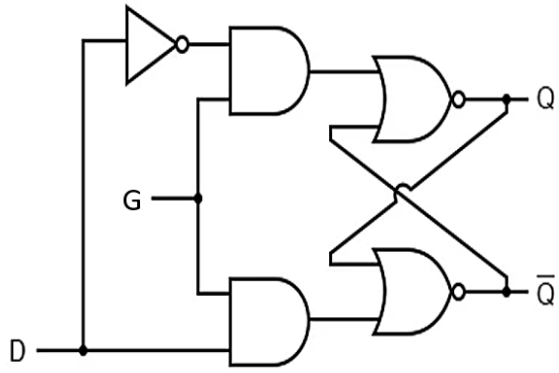
   (a)

A	B	Q(t)	Q(t+ϵ)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

   (b) Q(t+ϵ) = AQ' + BQ

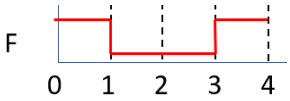
   Each wrong term would deduct 8 points
   Not minimize the equation would deduct 4 points.
   e.g. Q(t+ϵ) = BQ + AQ + AB would deduct (8+4) points

2. (60%) The circuit is shown below:



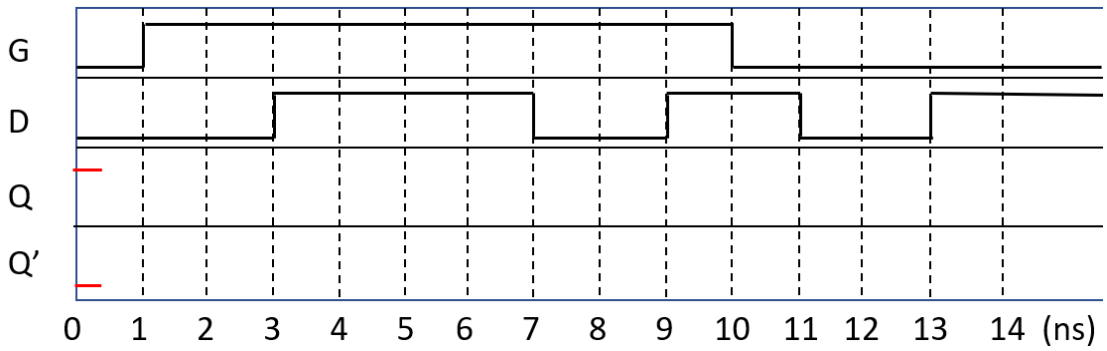
Complete the following timing diagram (Q and Q'), assuming initial Q=1, Q'=0 and each AND gate, NOR gate, and invertor has the same propagation delay 1ns.

Please use 0/1 to represent the timing diagram. If signal is 1 when time0 ~ time1, use 1 to represent it. For example, if one signal F is as follow:

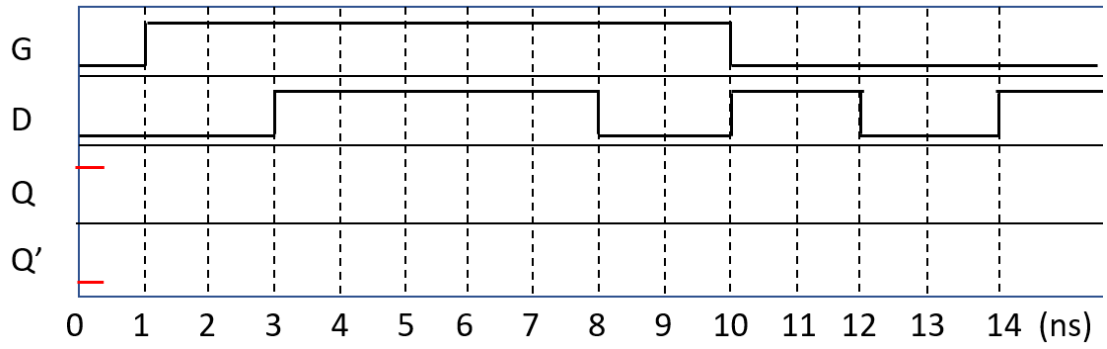


Please use "F: 1 0 0 1" to represent it.

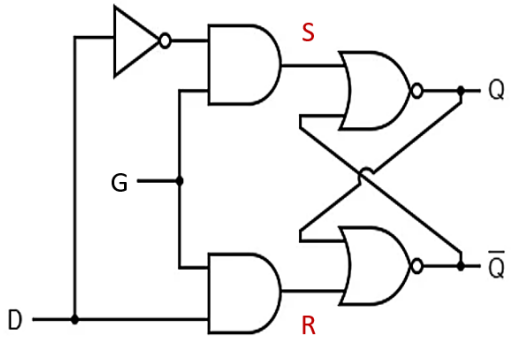
Question A:



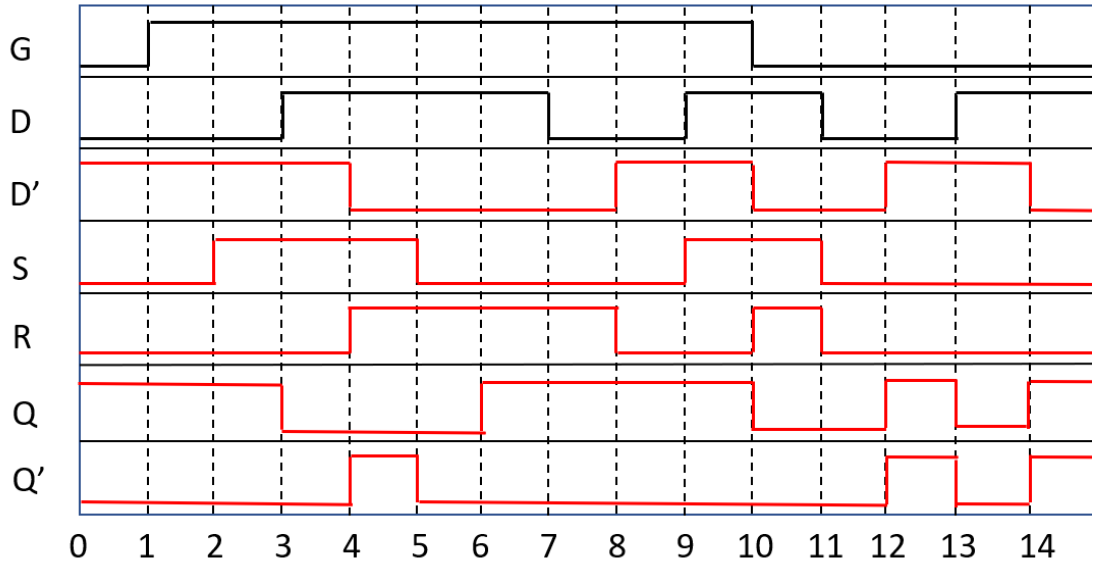
Question B:



Ans: (each wrong signal would deduct 2 points)



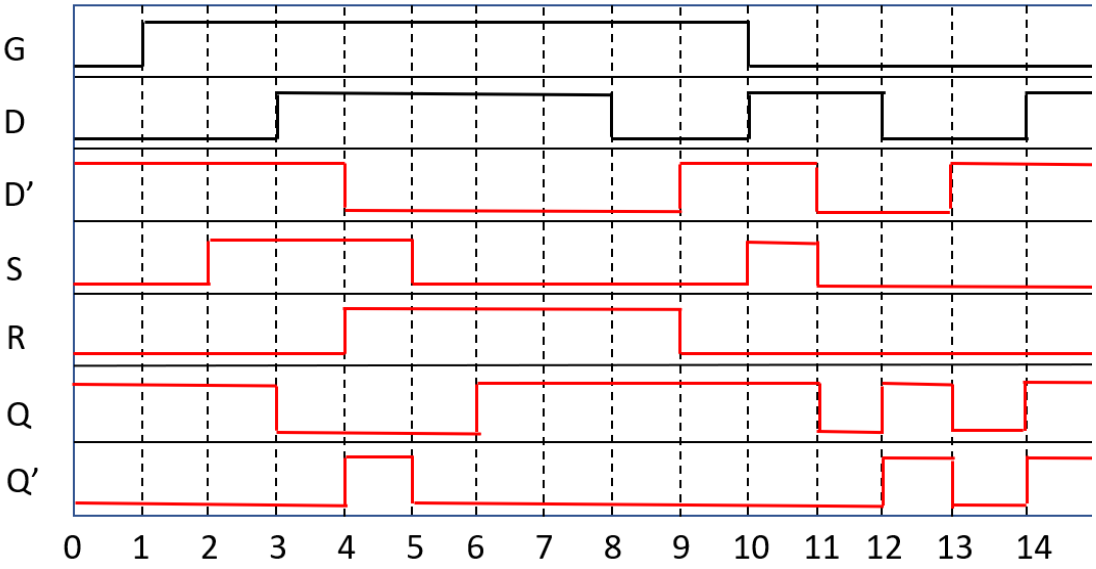
Question A



Q: 1 1 1 0 0 0 1 1 1 1 0 0 1 0 (1)

Q': 0 0 0 0 1 0 0 0 0 0 0 0 1 0 (1)

Question B



Q: 1 1 1 0 0 0 1 1 1 1 1 0 1 0 (1)

Q': 0 0 0 0 1 0 0 0 0 0 0 0 1 0 (1)