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Logic design (Fall 2021)
Quiz # 14

Name:_____ID:_____

1. (100%) Derive the state table for the following Moore machine containing one input (X) and one output (Z). Z=1 if and only if the previous 4 inputs were 0111, 1011, 1100, 1111 / 0000, 0011, 0100, 1000; otherwise, Z=0. Assume that in the reset state all previous inputs were 0.
   (a). (50%) Complete the following state table with the given description of e ach state.
   (b). (50%) Complete the following state table with the given description of e ach state. (Eight states are sufficient.)

Ans:

(a).

State	Next State		Z	State Description
	X=0	X=1		
S0	S0	S1	0	Previous 4 bits: 0000
S1	S2	S3	0	Previous 4 bits: 0001
S2	S4	S5	0	Previous 4 bits: 0010
S3	S6	S7	0	Previous 4 bits: 0011
S4	S8	S9	0	Previous 4 bits: 0100
S5	S10	S11	0	Previous 4 bits: 0101
S6	S12	S13	0	Previous 4 bits: 0110
S7	S14	S15	1	Previous 4 bits: 0111
S8	S0	S1	0	Previous 4 bits: 1000
S9	S2	S3	0	Previous 4 bits: 1001
S10	S4	S5	0	Previous 4 bits: 1010
S11	S6	S7	1	Previous 4 bits: 1011
S12	S8	S9	1	Previous 4 bits: 1100
S13	S10	S11	0	Previous 4 bits: 1101
S14	S12	S13	0	Previous 4 bits: 1110
S15	S14	S15	1	Previous 4 bits: 1111

(b).

State	Next State		Z	State Description
	X=0	X=1		
S0	S0	S1	0	Previous 4 bits: -000, 0-00
S1	S4	S5	0	Previous 4 bits: -001
S2	S7	S2	1	Previous 4 bits: -111, 1011
S3	S0	S1	1	Previous 4 bits: 1100
S4	S0	S6	0	Previous 4 bits: -010
S5	S7	S2	0	Previous 4 bits: 0011
S6	S4	S2	0	Previous 4 bits: -101
S7	S3	S6	0	Previous 4 bits: -110

Ans:

(a).

State	Next State		Z	State Description
	X=0	X=1		
S0	S0	S1	1	Previous 4 bits: 0000
S1	S2	S3	0	Previous 4 bits: 0001
S2	S4	S5	0	Previous 4 bits: 0010
S3	S6	S7	1	Previous 4 bits: 0011
S4	S8	S9	1	Previous 4 bits: 0100
S5	S10	S11	0	Previous 4 bits: 0101
S6	S12	S13	0	Previous 4 bits: 0110
S7	S14	S15	0	Previous 4 bits: 0111
S8	S0	S1	1	Previous 4 bits: 1000
S9	S2	S3	0	Previous 4 bits: 1001
S10	S4	S5	0	Previous 4 bits: 1010
S11	S6	S7	0	Previous 4 bits: 1011
S12	S8	S9	0	Previous 4 bits: 1100
S13	S10	S11	0	Previous 4 bits: 1101
S14	S12	S13	0	Previous 4 bits: 1110
S15	S14	S15	0	Previous 4 bits: 1111

(b).

State	Next State		Z	State Description
	X=0	X=1		
S0	S0	S1	1	Previous 4 bits: -000, 0-00
S1	S2	S3	0	Previous 4 bits: -001
S2	S0	S4	0	Previous 4 bits: -010
S3	S5	S6	1	Previous 4 bits: 0011
S4	S2	S6	0	Previous 4 bits: -101
S5	S7	S4	0	Previous 4 bits: -110
S6	S5	S6	0	Previous 4 bits: -111, 1011
S7	S0	S1	0	Previous 4 bits: 1100