UNIT 11
LATCHES AND FLIP-FLOPS
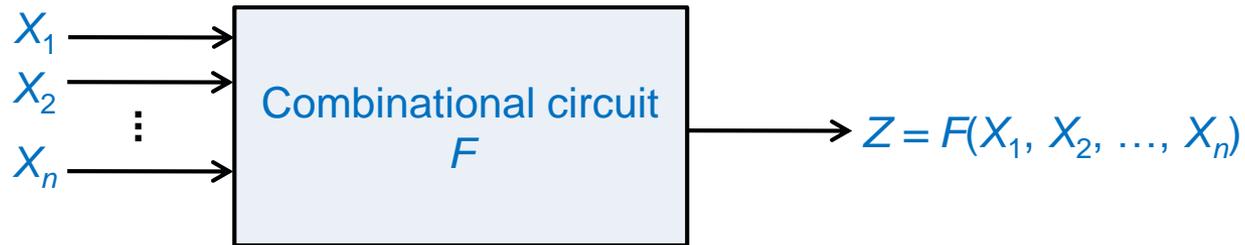
Fall 2021

Latches and Flip-Flops

- **Contents**
  - Set-Reset latch
  - Gated D latch
  - Edge-triggered D flip-flop
  - S-R flip-flop
  - J-K flip-flop
  - T flip-flop
  - Flip-flops with additional inputs
- **Reading**
  - Unit 11
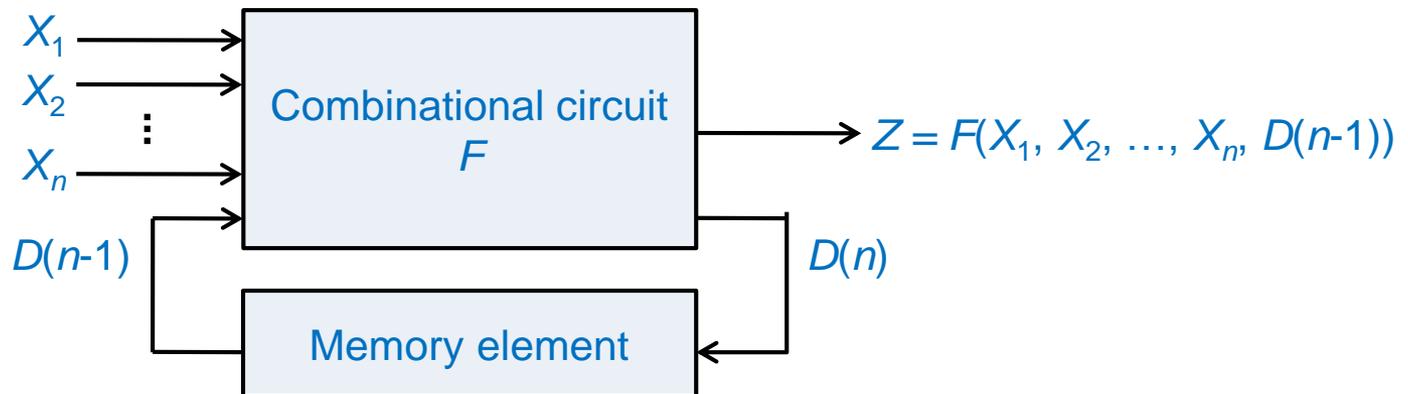
Recap: Two Types of Switching Circuits

- **Combinational circuits (memoryless)**
  - Outputs depend only on present inputs

X_1
X_2
⋮
X_n → Combinational circuit F → $Z = F(X_1, X_2, …, X_n)$

- **Sequential circuits (with memory)**
  - Outputs depend on both present & past inputs
  - In general, sequential ckts = combinational ckts + memory

X_1
X_2
⋮
X_n → Combinational circuit F → $Z = F(X_1, X_2, …, X_n, D(n\text{-}1))$

$D(n\text{-}1)$ Memory element $D(n)$
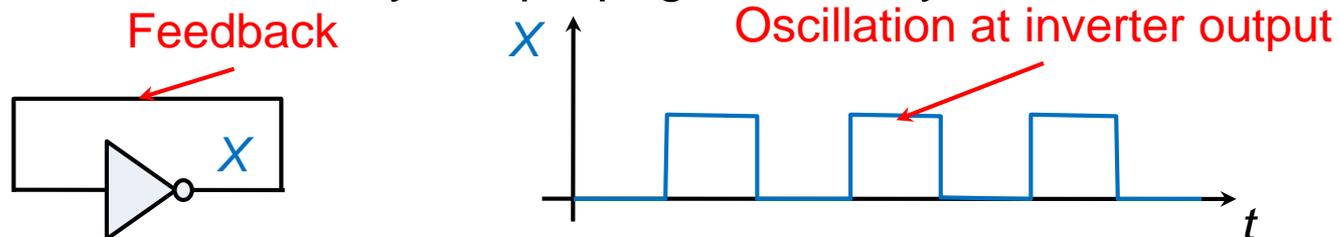
Latches & FFs

How to Remember the Past?

- **Feedback: the output of one of the gates is connected back into the input of another gate in the ckt so as to form a closed loop**
  - e.g., inverter with feedback
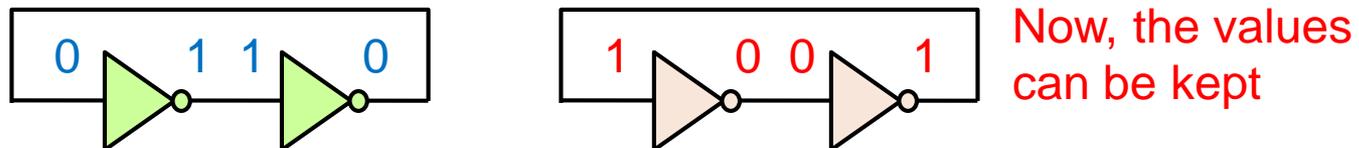   - Q: How fast does the circuit oscillate?
    - A: Determined by the propagation delay of the inverter

  Feedback X Oscillation at inverter output

  X

  t

  - e.g., a feedback loop with two inverters
    - Two stable states
    - Latch: basic memory unit (store 1 bit)

  0   1 1   0   1   0 0   1   Now, the values
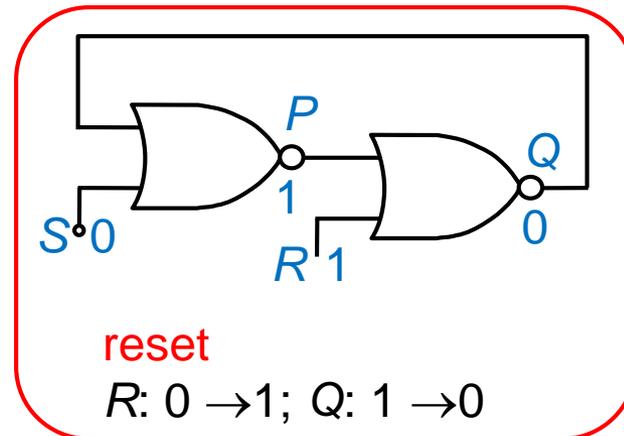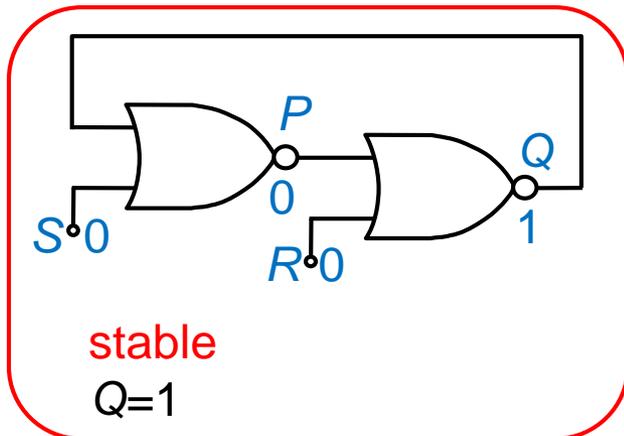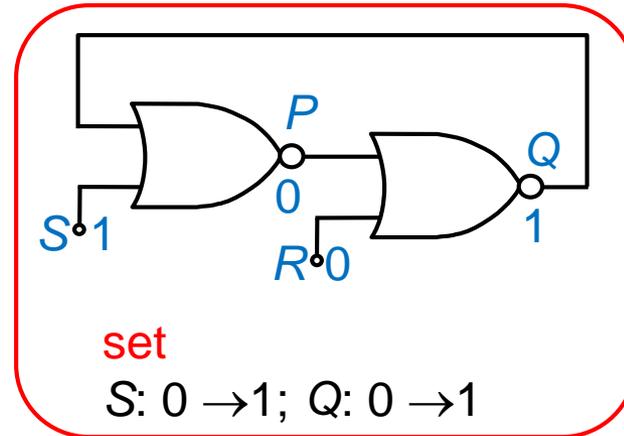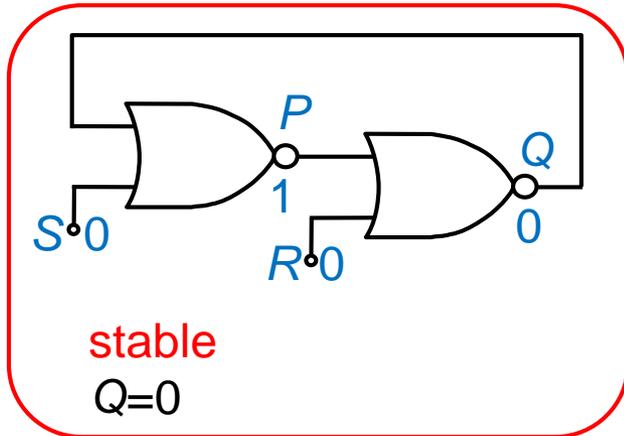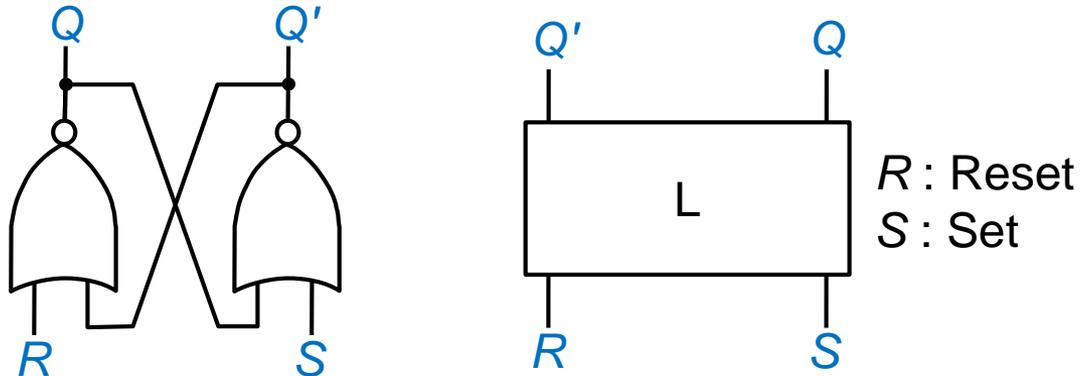   can be kept

5 Set-Reset Latch

S-R latch

Set-Reset (S-R) Latch (1/2)

stable
$Q=0$

set
$S: 0 \rightarrow 1; \; Q: 0 \rightarrow 1$

stable
$Q=1$

reset
$R: 0 \rightarrow 1; \; Q: 1 \rightarrow 0$

$P = Q'$

Latches & FFs

S-R Latch (2/2)

☐ **Cross-coupled form**

Q Q'

Q' Q

L

R : Reset
S : Set

R S

R S

☐ **S = R = 1 $\Rightarrow$ Unstable! Not allowed!!**

$1 \rightarrow 0$

S

P $0 \rightarrow 1 \rightarrow 0 \rightarrow 1...$

$P \neq Q'$

R

Q $0 \rightarrow 1 \rightarrow 0 \rightarrow 1...$

$1 \rightarrow 0$

Latches & FFs
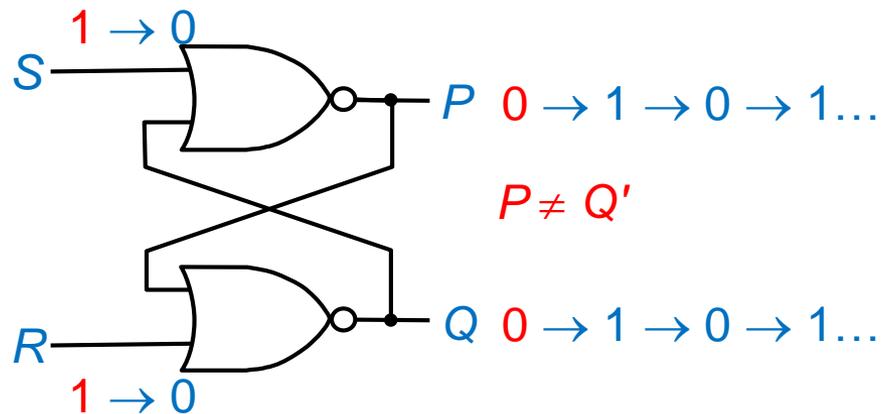
Next-State Equation

□ **Timing diagram**

ϵ: 2 gate delay
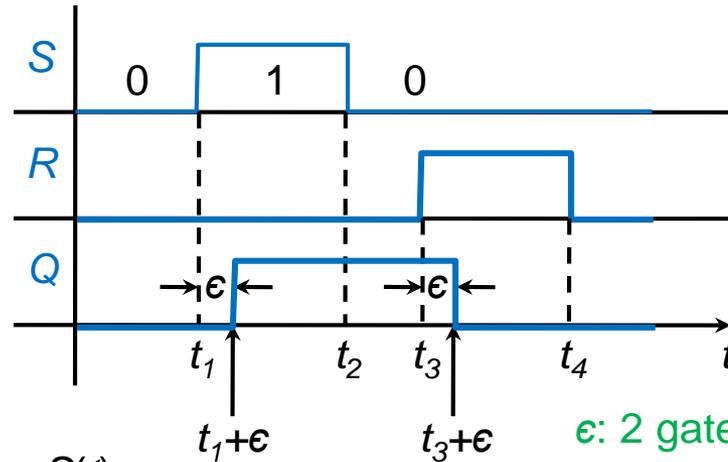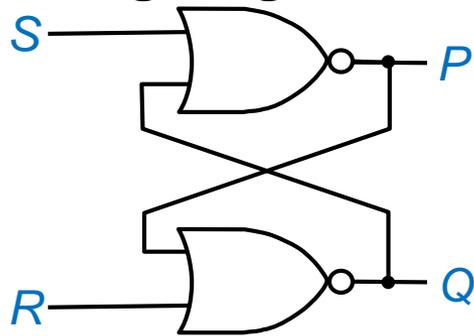
□ **Operation**

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\epsilon)$	
0	0	0	0	} Unchanged
0	0	1	1	
0	1	0	0	} Reset to 0
0	1	1	0	
1	0	0	1	} Set to 1
1	0	1	1	
1	1	0	–	} Inputs not allowed
1	1	1	–	

Latches & FFs

K-map ⟹

$S(t)$

$R(t)Q(t)$	0	1
00	**0**	**1**
01	**1**	**1**
11	**0**	**X**
10	**0**	**X**
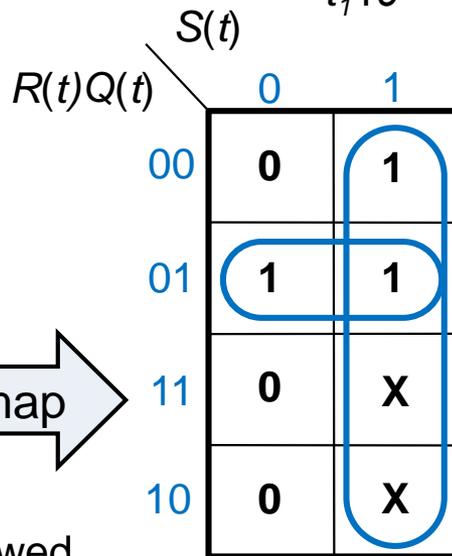
$Q(t+\epsilon)=S(t)+R'(t)\,Q(t)$

Next-state equation:
(Characteristic equation)

$Q^+ = S+R'Q$
under $SR=0$
($S=1$, $R=1$ not allowed)

Application: Switch Debouncing

- **When a mechanical switch is opened or closed, switch contacts tend to vibrate before settling down $\Rightarrow$ Debounce with S-R latch**
  - e.g, when the switch is flipped from *a* to *b*…
  - Work only with a "double throw" switch
    - Double throw: switch between two contacts
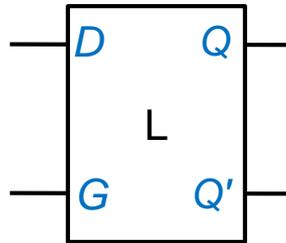   - Single throw: switch between one contact and open

S=R=0
Q unchanged

Pull down resistors

Switch at *a* Bounce at *a* Switch between *a* and *b* Bounce at *b* Switch at *b*
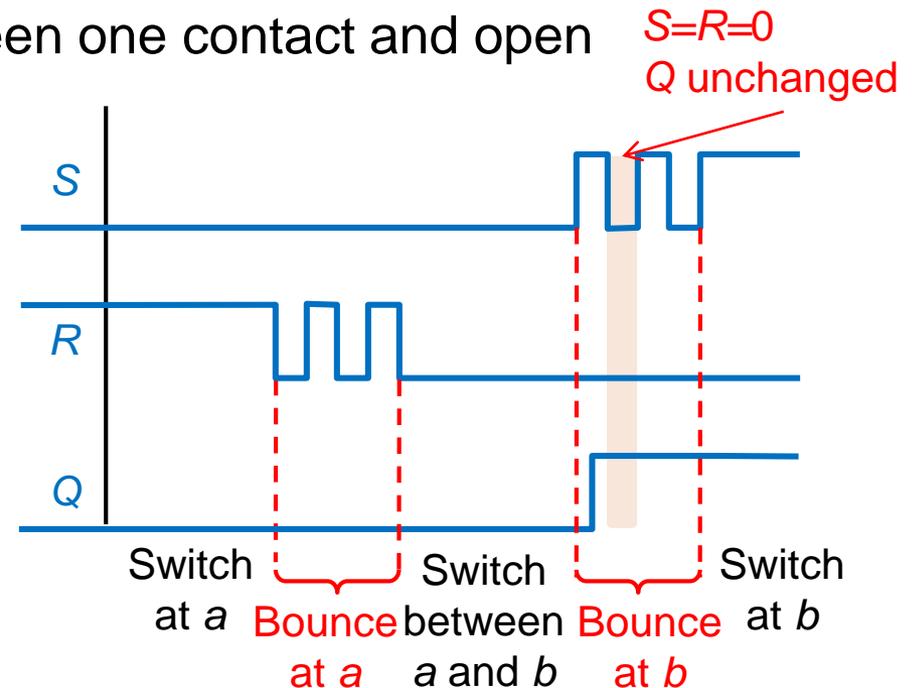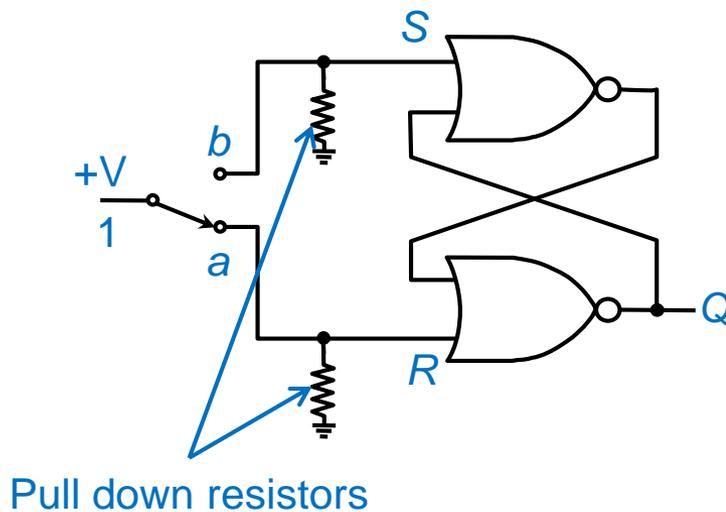
Alternative Form with NAND-Gates

□ **$\overline{S}$-$\overline{R}$ latch: active-low inputs for *S* & *R***
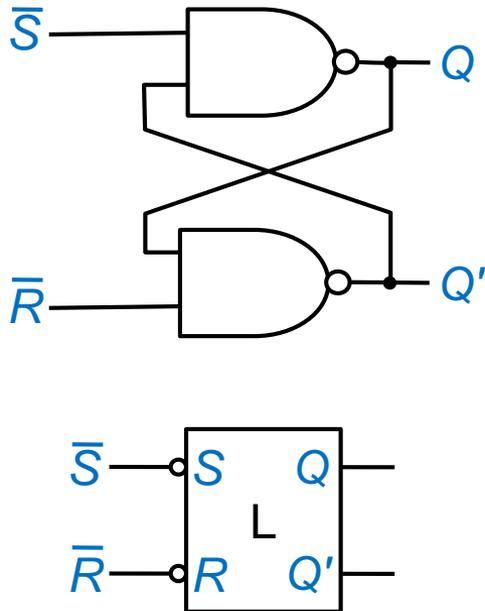
$\overline{S}$	$\overline{R}$	Q	Q^+	
1	1	0	0	} Unchanged
1	1	1	1	
1	0	0	0	} Reset to 0
1	0	1	0	
0	1	0	1	} Set to 1
0	1	1	1	
0	0	0	−	} Inputs not allowed
0	0	1	−	
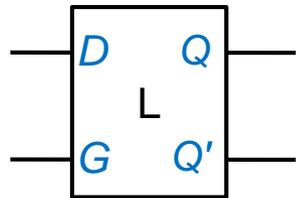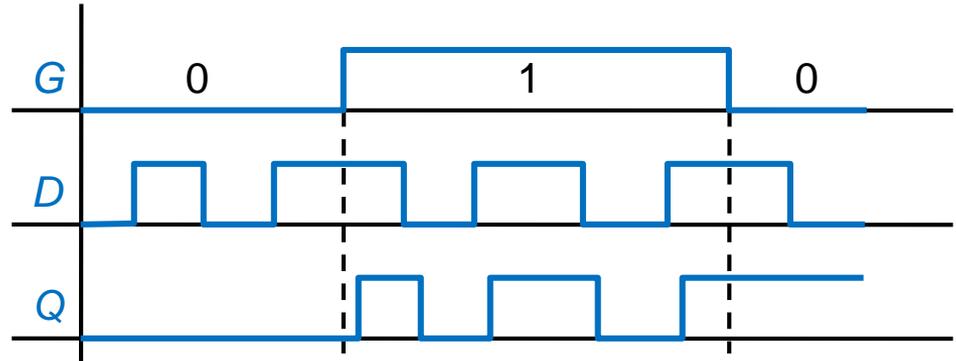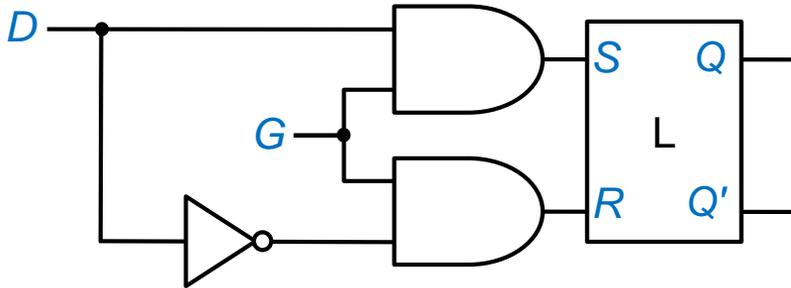
Latches & FFs

Gated D Latch

Latches & FFs

Gated D Latch

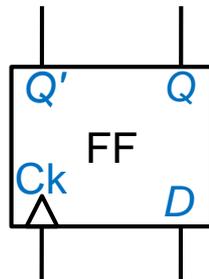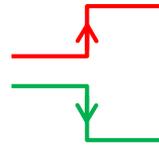| G	D	Q	Q⁺	
0	0	0	0	Unchanged $Q^+ = Q$
0	0	1	1	
0	1	0	0	
0	1	1	1	
1	0	0	0	Update $Q^+ = D$
1	0	1	0	
1	1	0	1	
1	1	1	1	

$Q^+ = G'Q + GD$

Latches & FFs

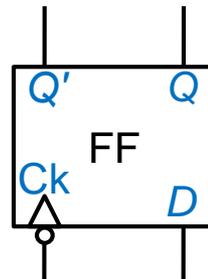# Edge-Triggered D Flip-Flop
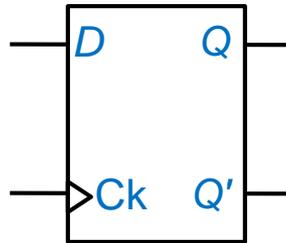
Edge-Triggered D Flip-Flops

□ **Output changes are aligned with clock edges**

  ▫ Positive (rising-edge) trigger
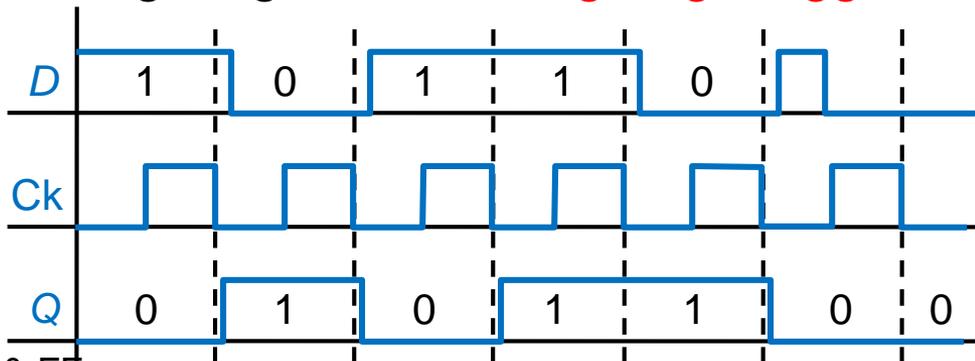
  ▫ Negative (falling-edge) trigger

  ▫ Symbol

  ▫ Truth table

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

$Q^+ = D$

Rising-edge trigger   Falling-edge trigger

  ▫ Timing diagram for falling-edge triggered D FF
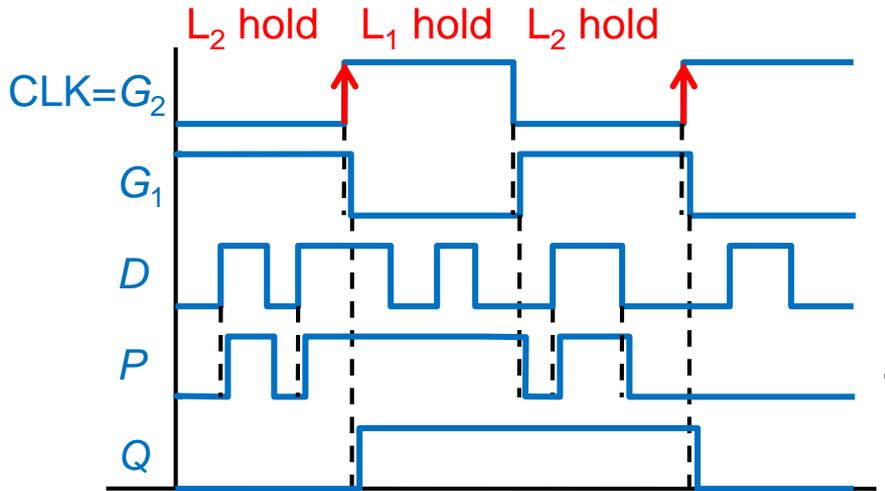

Latches & FFs

D FF – Rising Edge Trigger

□ **Construct from 2 gated D latches**
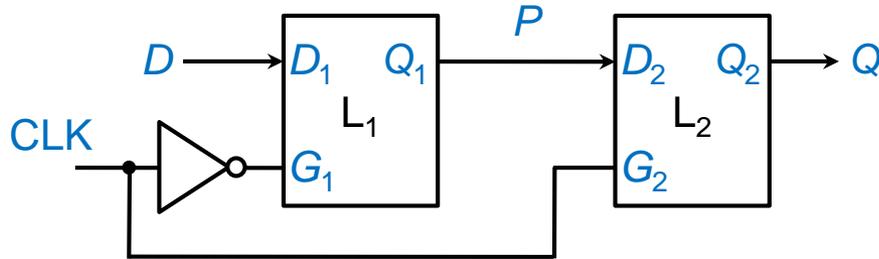
□ **Timing diagram (setup/hold time)**

Q: What's the difference between a latch and a FF?

The value of a flip-flop' output won't change during a clock cycle.

Latches & FFs

Timing of a D FF (Setup Time/Hold Time)

- Because a flip-flop changes state only on the active edge of the clock, the *propagation delay (t_p) of a flip-flop* is the time between the active edge of the clock and the resulting change in the output.

- To function properly, the D input to an edge-triggered flip-flop must be held at a constant value for a period of time before and after the active edge of the clock.

- The amount of time that D must be stable before the active edge is called the *setup time* (t_{su}), and the amount of time that D must hold the same value after the active edge is the *hold time* (t_h).
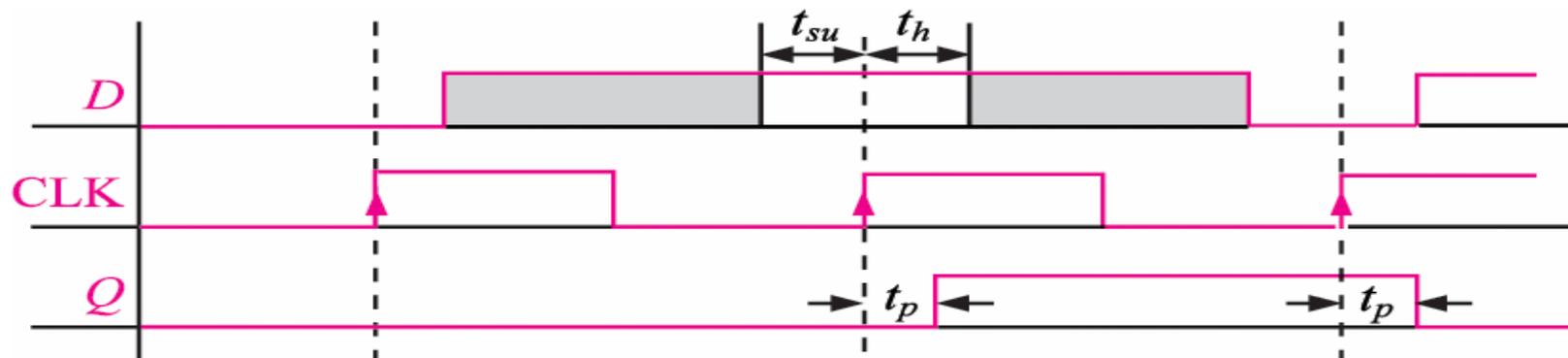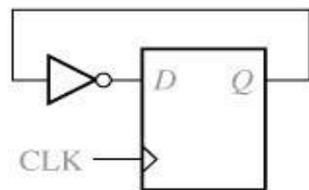
Minimum Clock Period

- **Determine the Minimum Clock Period**
  - Minimum clock period

    =(total delay of gates) + (delay of flip-flop + setup time)

- ## Example: Suppose that
  - Propagation delay of the inverter = 2*ns,*
  - Propagation delay of the D flip-flop = 5*ns,*
  - Setup time of the D Flip-flop = 3*ns.*
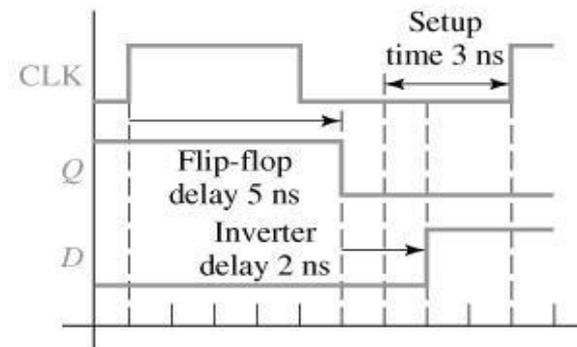
    Determine the minimum clock period of the circuit.
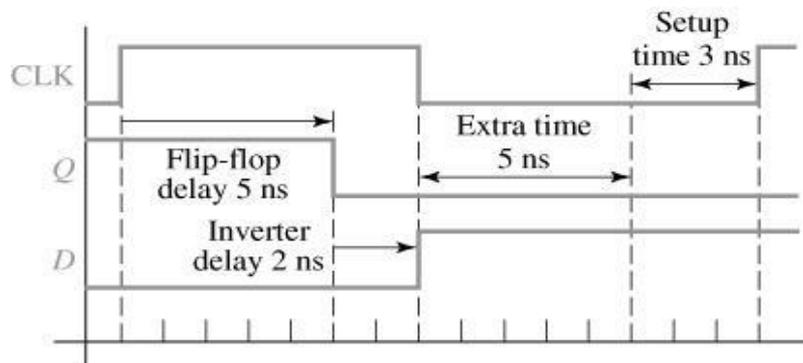
Latches & FFs

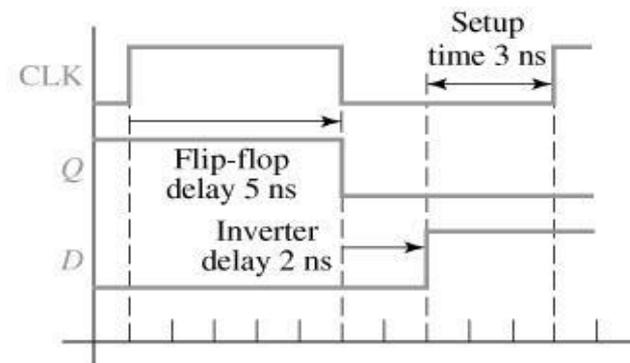# Edge-Triggered D Flip-Flop

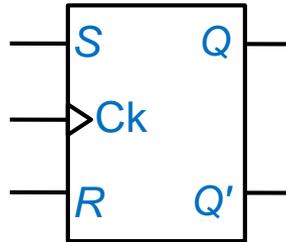❑ **Example (cont.):**

(a) Simple flip-flop circuit

(b) Setup time not satisfied
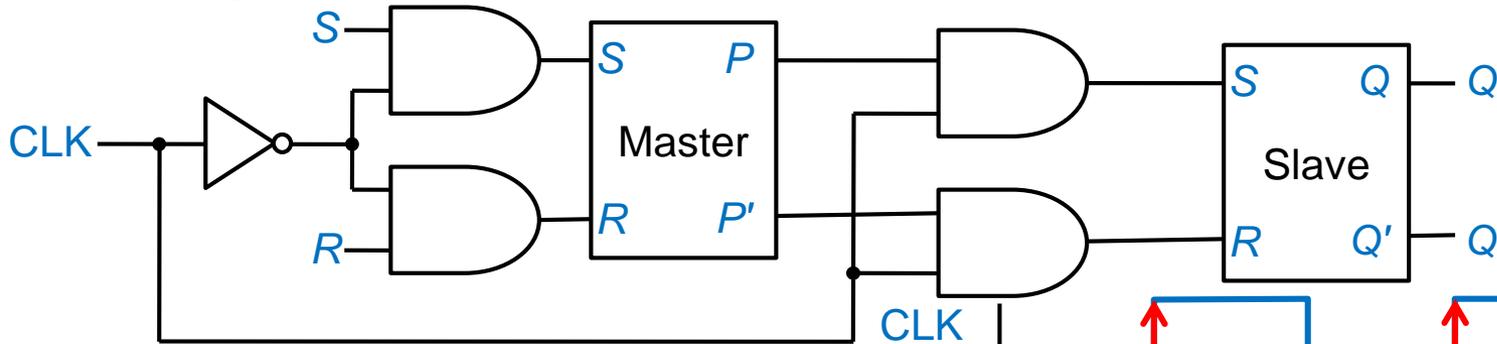
(c) Setup time satisfied

(d) Minimum clock period

Latches & FFs

S-R Flip-Flop

Latches & FFs

S-R Flip Flop

□ **Output changes at clock edges**
□ **Construct from 2 latches**
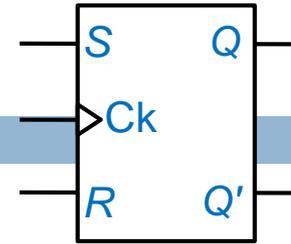
□ **Operation**

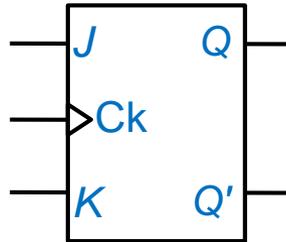| S	R	operation
0	0	No state change
0	1	Reset Q to 0 (after active Ck edge)
1	0	Set Q to 1 (after active Ck edge)
1	1	Not allowed
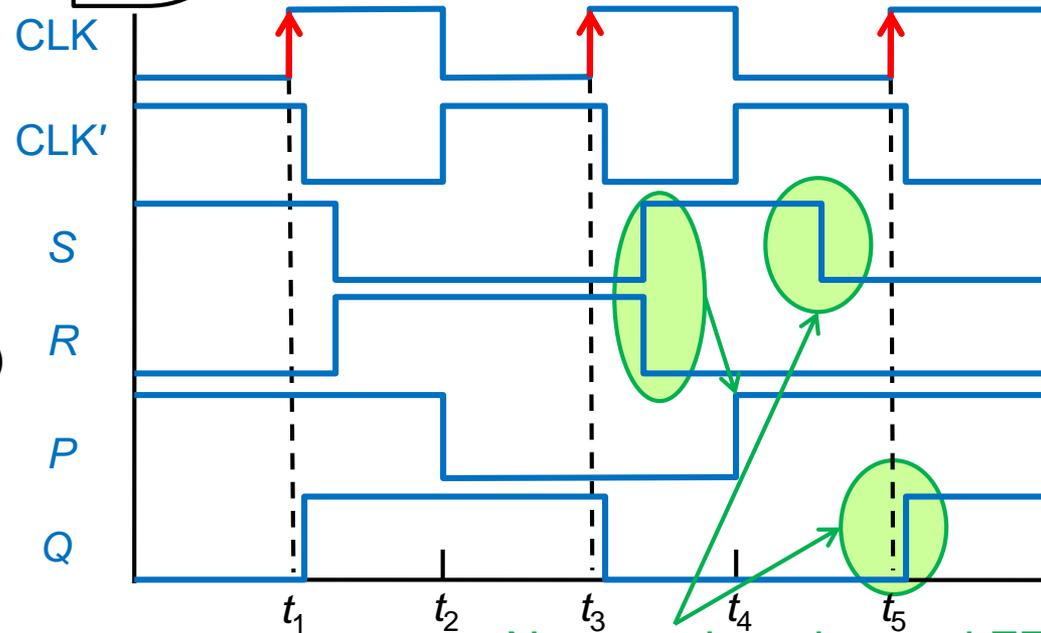
Not an edge-triggered FF
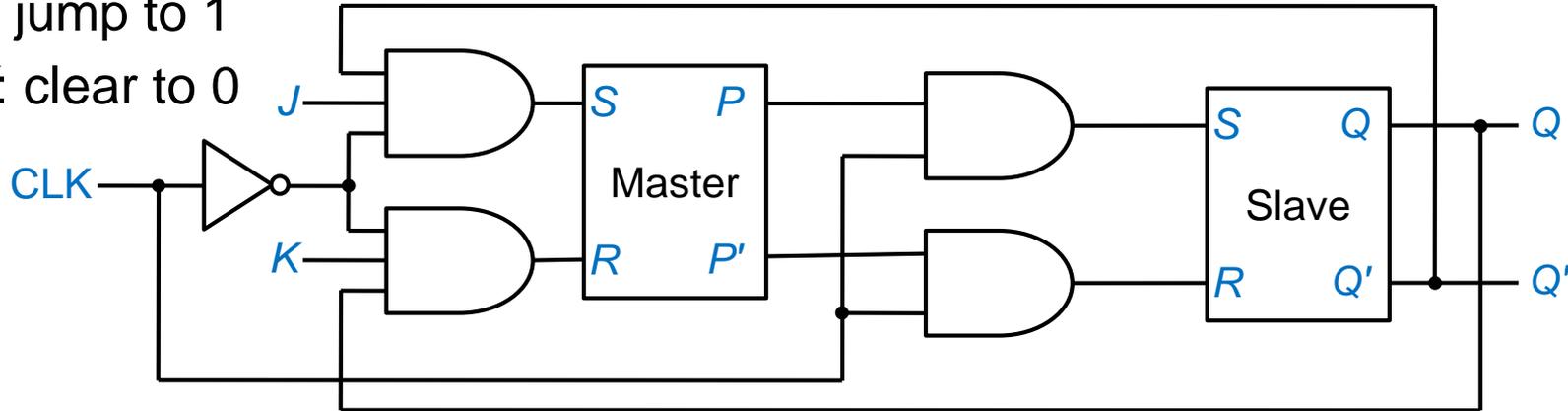⇒ Do not allow SR change while CLK is low

Latches & FFs

J-K Flip-Flop

J-K Flip-Flop
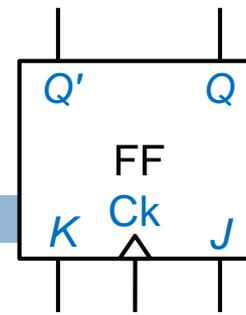
□ **Extension of S-R FF**

- J: jump to 1
- K: clear to 0

J	K	Q	Q+	
0	0	0	0	Unchanged
0	0	1	1	
0	1	0	0	Clear to 0
0	1	1	0	
1	0	0	1	Jump to 1
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	
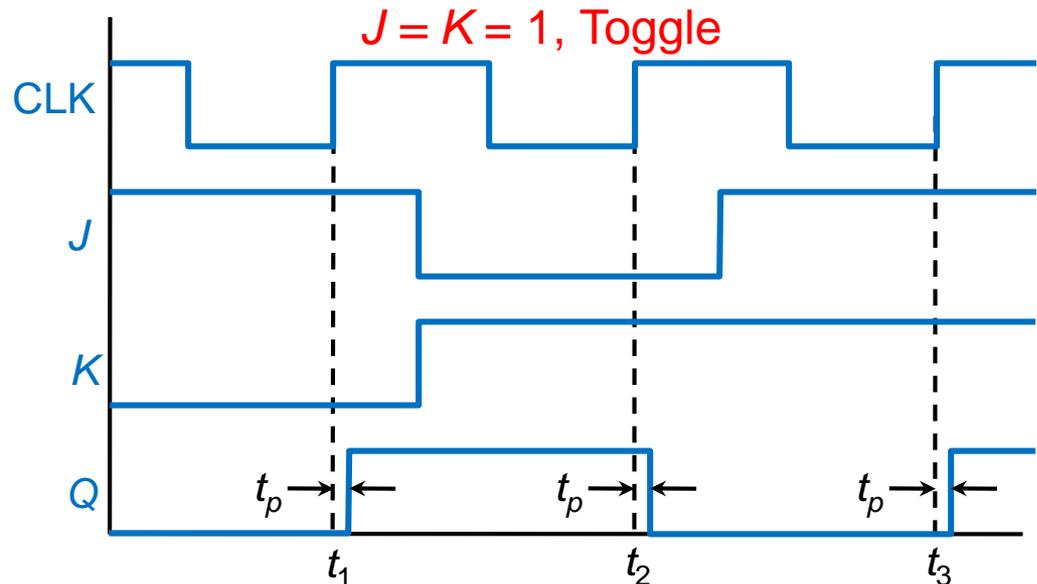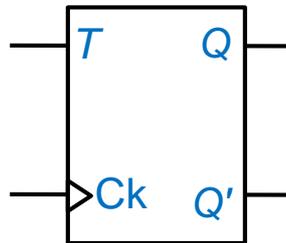
$Q^+ = JQ' + K'Q$

$J = K = 1$, Toggle

T Flip-Flop

T Flip-Flop

© Iris H.-R. Jiang

□ **T: Toggle**

T	Q	$Q^+=T'Q+TQ'=T\oplus Q$	
0	0	0	} Unchanged
0	1	1	
1	0	1	} Toggle
1	1	0	
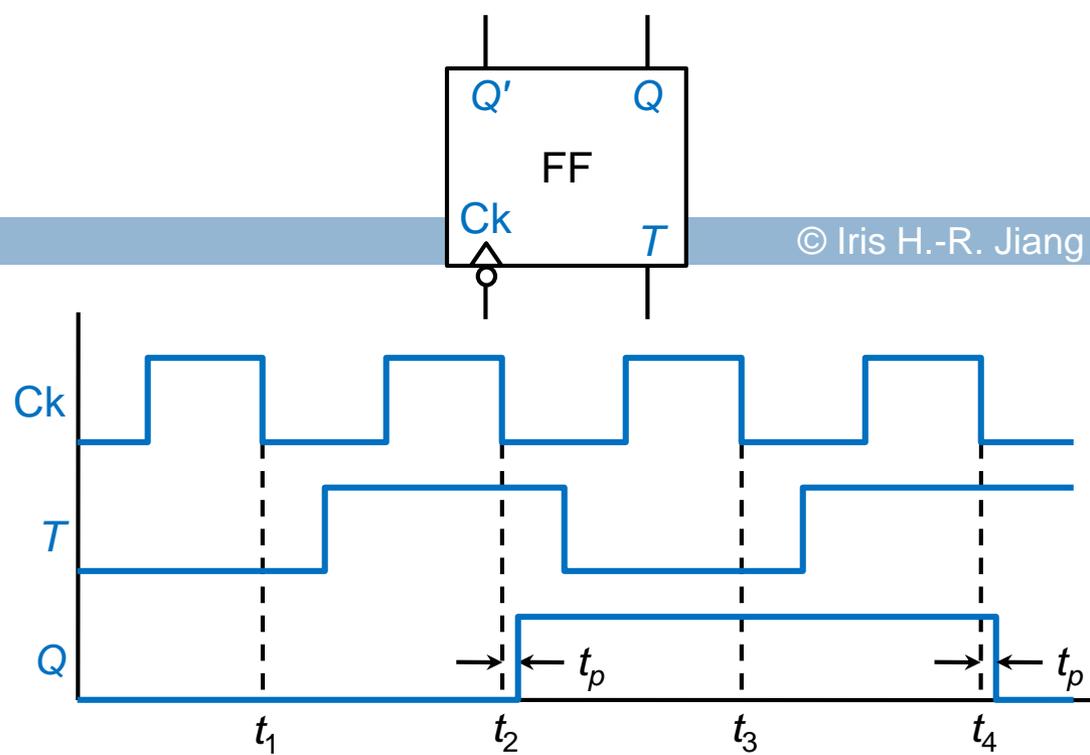
□ **Implementation**
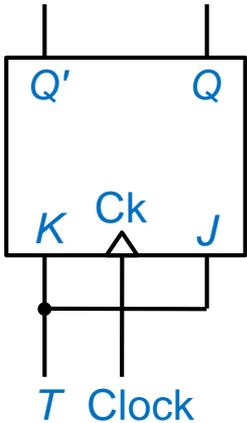
J-K FF based:
$J = K = 0$ Unchanged
$J = K = 1$ Toggle
$Q^+ = JQ' + K'Q$
$\quad = TQ' + T'Q$
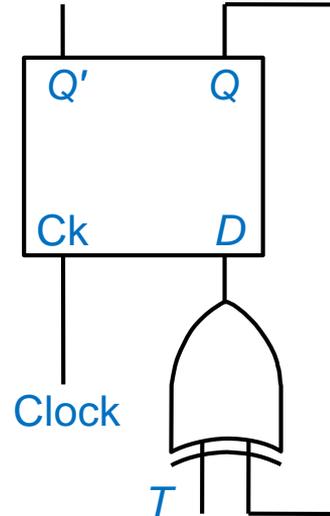
D FF based:
D input: $T\oplus Q$
$Q^+ = T\oplus Q$
$\quad = TQ' + T'Q$

Latches & FFs

25 FFs with Additional Inputs
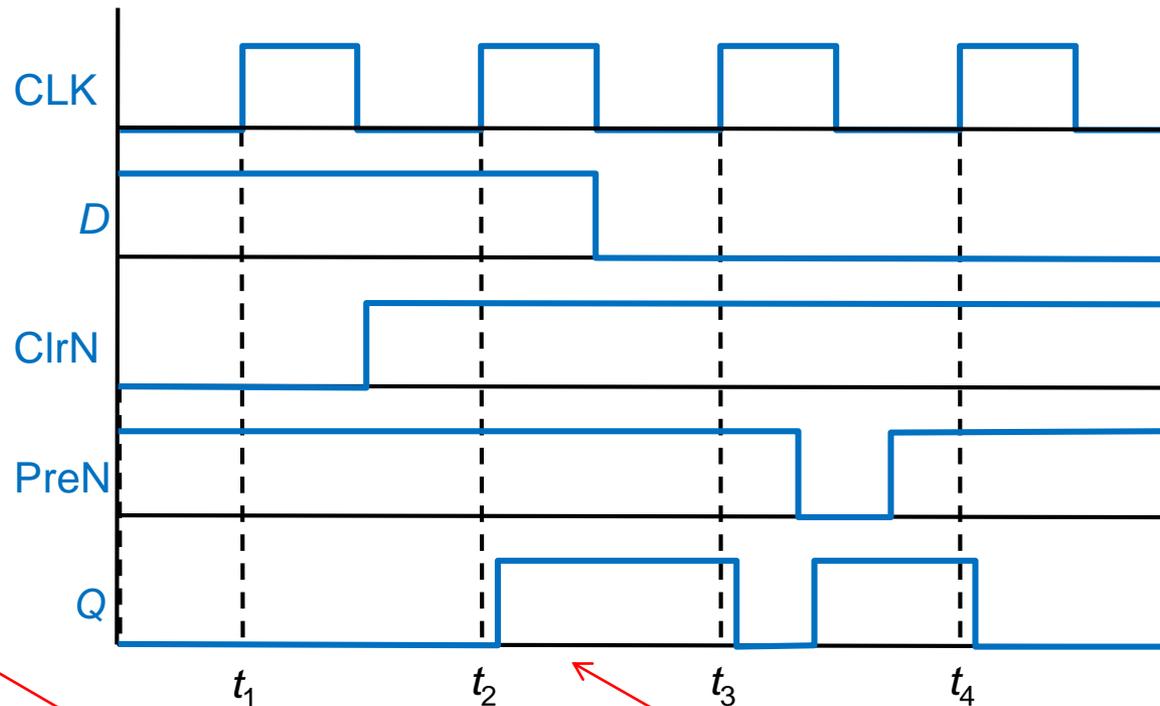
D FF with Clear and Preset

- **Use additional inputs to set FF to an initial state independent of the clock**

  - e.g., asynchronous Clear and Preset
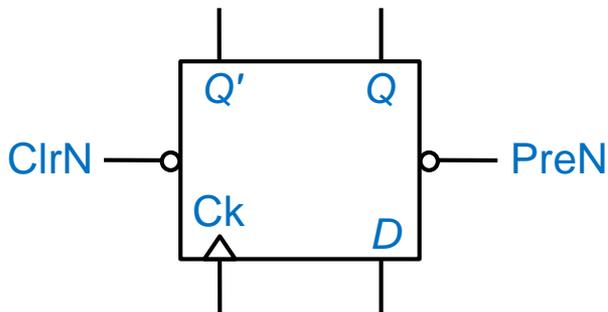
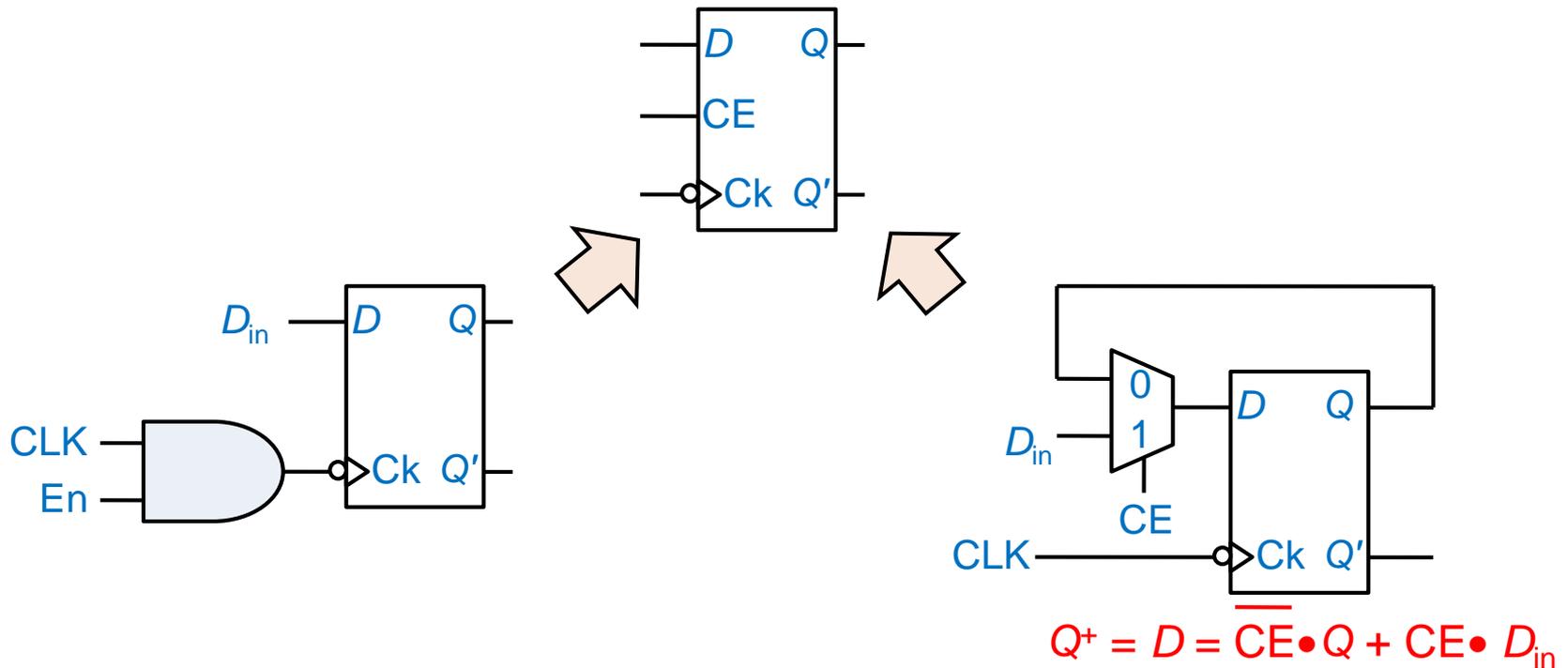| Ck	D	PreN	ClrN	Q⁺
x	x	0	0	- (not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1,↓	x	1	1	Q (no change)

Normal FF

Keep whole cycle

Latches & FFs

D FF with Clock Enable

- **We want some Flip-flops to hold existing data even though the data input may be changing**
  - Gated clock: gate the clock by clock enable (CE)

$$Q^+ = D = \overline{CE} \bullet Q + CE \bullet D_{in}$$

28 Summary

Latches & FFs

Characteristic Equations for Latches & FFs

Type	Q^+
S-R latch or FF	$Q^+ = S + R'Q \ (SR = 0)$
Gated D latch	$Q^+ = G'Q + GD$
D FF	$Q^+ = D$
D-CE FF	$Q^+ = D \bullet CE + Q \bullet CE'$
J-K FF	$Q^+ = JQ' + K'Q$
T FF	$Q^+ = T \oplus Q$