UNIT 16
SEQUENTIAL CIRCUIT DESIGN

Fall 2021

Sequential Circuit Design

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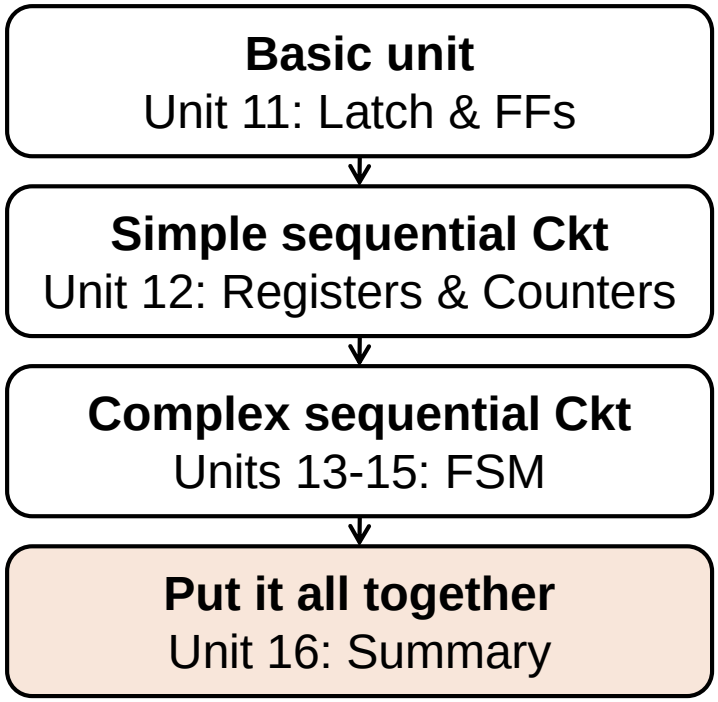

Designing a Sequential Circuit

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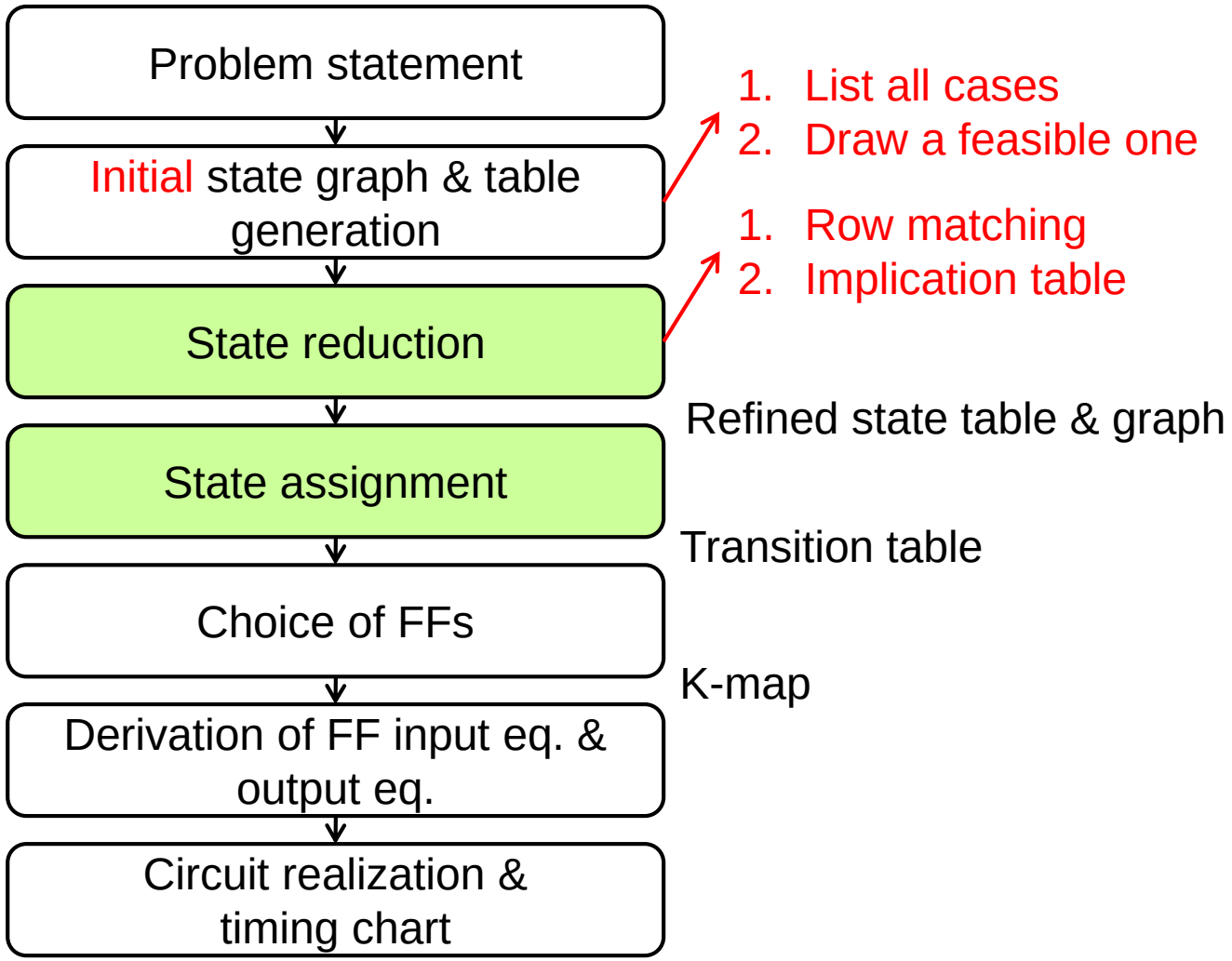

Design Example—Code Converter

BCD to Excess-3 Conversion

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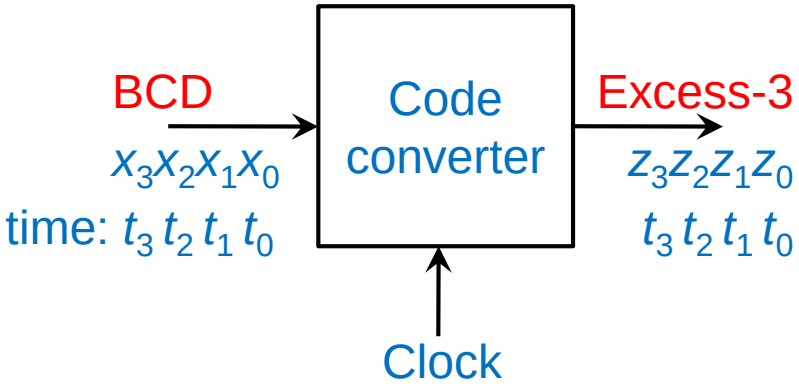
- **BCD ⇒ excess-3**
  - Add 3 to BCD (0~9)
  - Serial I/O with the LSB first
    - $x_0 \rightarrow x_1 \rightarrow x_2 \rightarrow x_3$
    - $z_0 \rightarrow z_1 \rightarrow z_2 \rightarrow z_3$
  - Reset to initial state after receiving 4 inputs



X Input (BCD)	Z Output (excess-3)
time: $t_3\,t_2\,t_1\,t_0$	$t_3\,t_2\,t_1\,t_0$
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0
(1010~1111)	x x x x

Serial Code Conversion (1/8)

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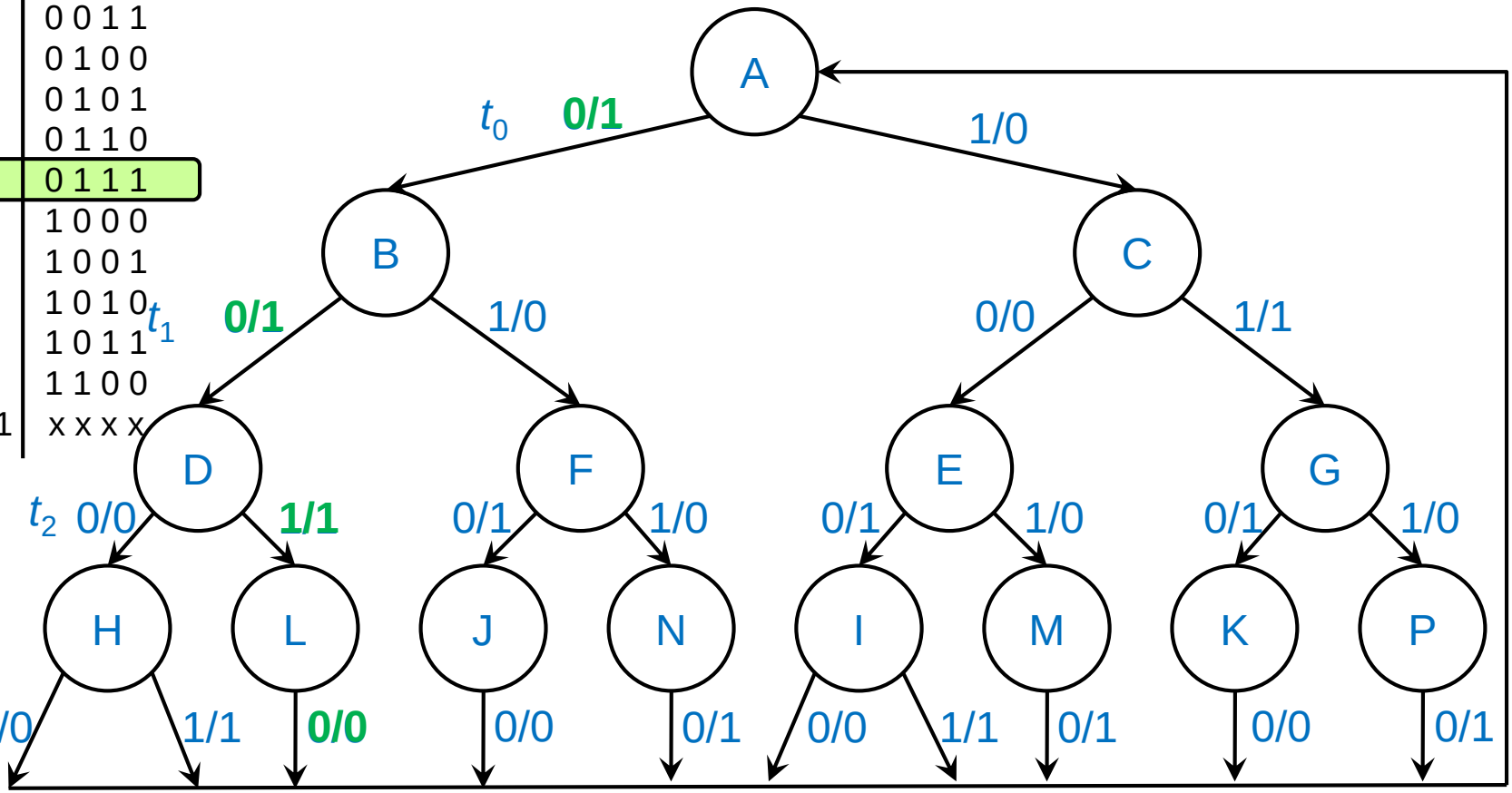
- **State graph: list all cases**

X Input (BCD) time: $t_3\,t_2\,t_1\,t_0$	*Z* Output (excess-3) $t_3\,t_2\,t_1\,t_0$
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0
1010~1111	x x x x



Serial Code Conversion (2/8)

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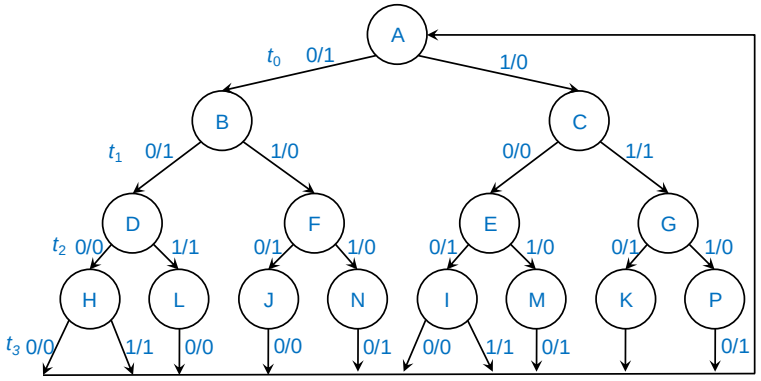
- **State table**

time	Input sequence (LSB first)	Present state	Next state $X=0$	Next state $X=1$	Present Output (Z) $X=0$	Present Output (Z) $X=1$
t_0	reset	*A*	*B*	*C*	1	0
t_1	0	*B*	*D*	*F*	1	0
	1	*C*	*E*	*G*	0	1
t_2	00	*D*	*H*	*L*	0	1
	01	*E*	*I*	*M*	1	0
	10	*F*	*J*	*N*	1	0
	11	*G*	*K*	*P*	1	0
t_3	000	*H*	*A*	*A*	0	1
	001	*I*	*A*	*A*	0	1
	010	*J*	*A*	-	0	-
	011	*K*	*A*	-	0	-
	100	*L*	*A*	-	0	-
	101	*M*	*A*	-	1	-
	110	*N*	*A*	-	1	-
	111	*P*	*A*	-	1	-



Serial Code Conversion (3/8)

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- **State reduction**
  - Row matching
  - Use don't cares
    - $M \equiv N \equiv P$
    - $H \equiv I \equiv J \equiv K \equiv L$
    - $E \equiv F \equiv G$

time	Input sequence (LSB first)	Present state	Next state $X=0$	Next state $X=1$	Present Output (Z) $X=0$	Present Output (Z) $X=1$
t_0	reset	A	B	C	1	0
t_1	0	B	D	E F	1	0
	1	C	E	E G	0	1
t_2	00	D	H	H L	0	1
	01	E	H I	M	1	0
	10	F	H J	M N	1	0
	11	G	H K	M P	1	0
t_3	000	H	A	A	0	1
	001	I	A	A	0	1
	010	J	A	-	0	-
	011	K	A	-	0	-
	100	L	A	-	0	-
	101	M	A	-	1	-
	110	N	A	-	1	-
	111	P	A	-	1	-

Serial Code Conversion (4/8)

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- **Reduced state table**
  - 7 states

time	Present state	Next state $X=0$	Next state $X=1$	Present Output (Z) $X=0$	Present Output (Z) $X=1$
t_0	A	B	C	1	0
t_1	B	D	E	1	0
	C	E	E	0	1
t_2	D	H	H	0	1
	E	H	M	1	0
t_3	H	A	A	0	1
	M	A	-	1	-

Serial Code Conversion (5/8)

- **State assignment**
  - 7 states ⇒ 3 FFs

time	Present state	Next state $X=0$	Next state $X=1$	Output (Z) $X=0$	Output (Z) $X=1$
t_0	A	B	C	1	0
t_1	B	D	E	1	0
	C	E	E	0	1
t_2	D	H	H	0	1
	E	H	M	1	0
t_3	H	A	A	0	1
	M	A	-	1	-

  - ⇒ Transition table

	$Q_1Q_2Q_3$	$Q_1^+Q_2^+Q_3^+$ $X=0$	$Q_1^+Q_2^+Q_3^+$ $X=1$	Z $X=0$	Z $X=1$
A	0 0 0	1 0 0	1 0 1	1	0
B	1 0 0	1 1 1	1 1 0	1	0
C	1 0 1	1 1 0	1 1 0	0	1
D	1 1 1	0 1 1	0 1 1	0	1
E	1 1 0	0 1 1	0 1 0	1	0
H	0 1 1	0 0 0	0 0 0	0	1
M	0 1 0	0 0 0	x x x	1	x
-	0 0 1	x x x	x x x	x	x

Q_2Q_3 \ Q_1	0	1
00	A	B
01		C
11	H	D
10	M	E

(6/8)

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- **Choose D FFs**
- **Derive FF input eq. & output eq.**

		$Q_1^+Q_2^+Q_3^+$		Z	
	$Q_1Q_2Q_3$	$X=0$	$X=1$	$X=0$	$X=1$
A	0 0 0	1 0 0	1 0 1	1	0
B	1 0 0	1 1 1	1 1 0	1	0
C	1 0 1	1 1 0	1 1 0	0	1
D	1 1 1	0 1 1	0 1 1	0	1
E	1 1 0	0 1 1	0 1 0	1	0
H	0 1 1	0 0 0	0 0 0	0	1
M	0 1 0	0 0 0	x x x	1	x
-	0 0 1	x x x	x x x	x	x

Q_2Q_3 \ XQ_1	00	01	11	10
00	1	1	1	1
01	x	1	1	x
11	0	0	0	0
10	0	0	0	x

$D_1=Q_1^+=Q_2'$

Q_2Q_3 \ XQ_1	00	01	11	10
00	0	1	1	0
01	x	1	1	x
11	0	1	1	0
10	0	1	1	x

$D_2=Q_2^+=Q_1$

(7/8)

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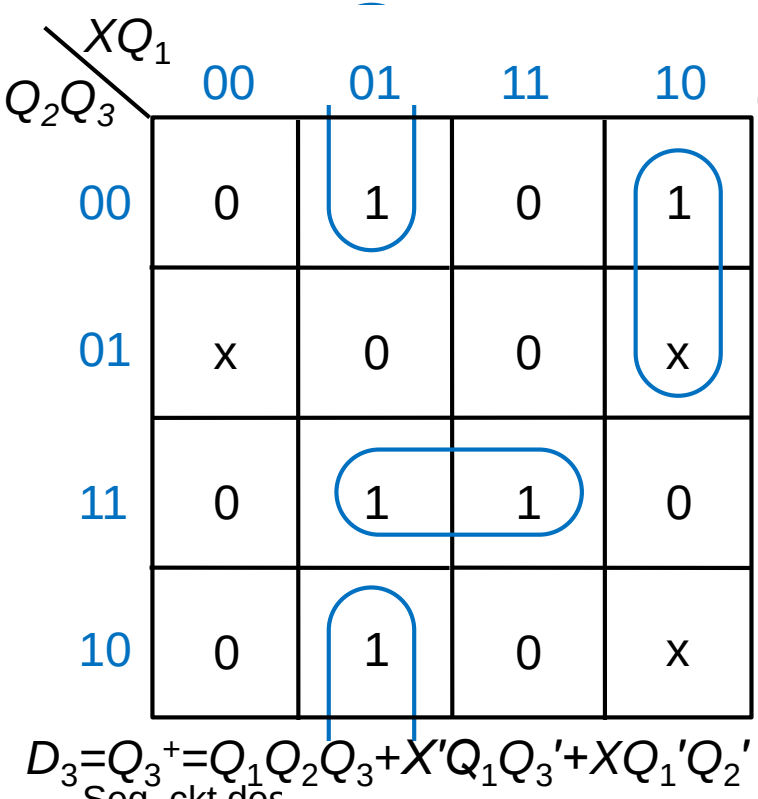
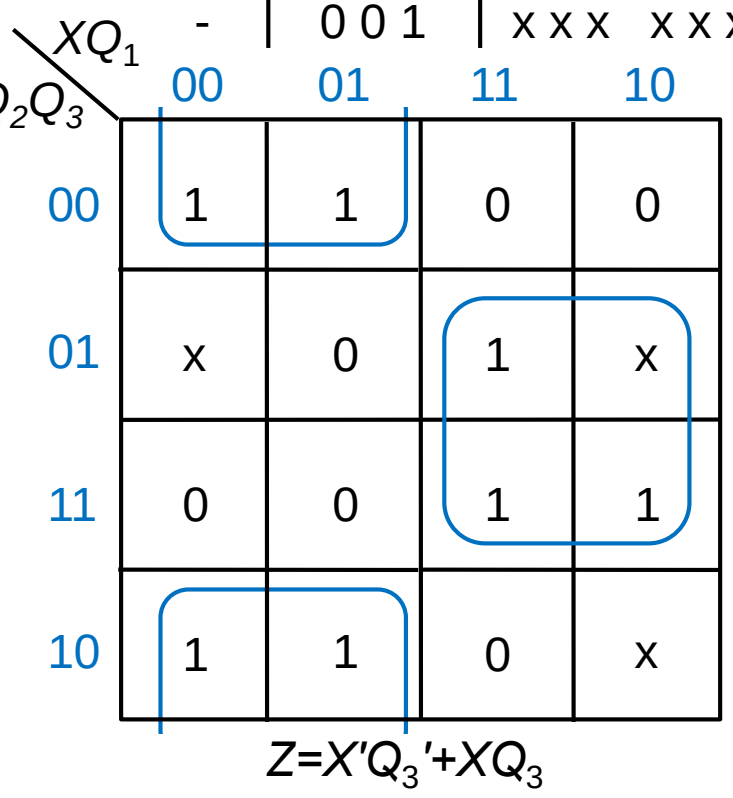
- **Choose D FFs**
- **Derive FF input eq. & output eq.**

		$Q_1^+Q_2^+Q_3^+$		Z	
	$Q_1Q_2Q_3$	$X=0$	$X=1$	$X=0$	$X=1$
A	0 0 0	1 0 0	1 0 1	1	0
B	1 0 0	1 1 1	1 1 0	1	0
C	1 0 1	1 1 0	1 1 0	0	1
D	1 1 1	0 1 1	0 1 1	0	1
E	1 1 0	0 1 1	0 1 0	1	0
H	0 1 1	0 0 0	0 0 0	0	1
M	0 1 0	0 0 0	x x x	1	x
-	0 0 1	x x x	x x x	x	x



$D_3=Q_3^+=Q_1Q_2Q_3+X'Q_1Q_3'+XQ_1'Q_2'$



$Z=X'Q_3'+XQ_3$

Seq. ckt des

Serial Code Conversion (8/8)

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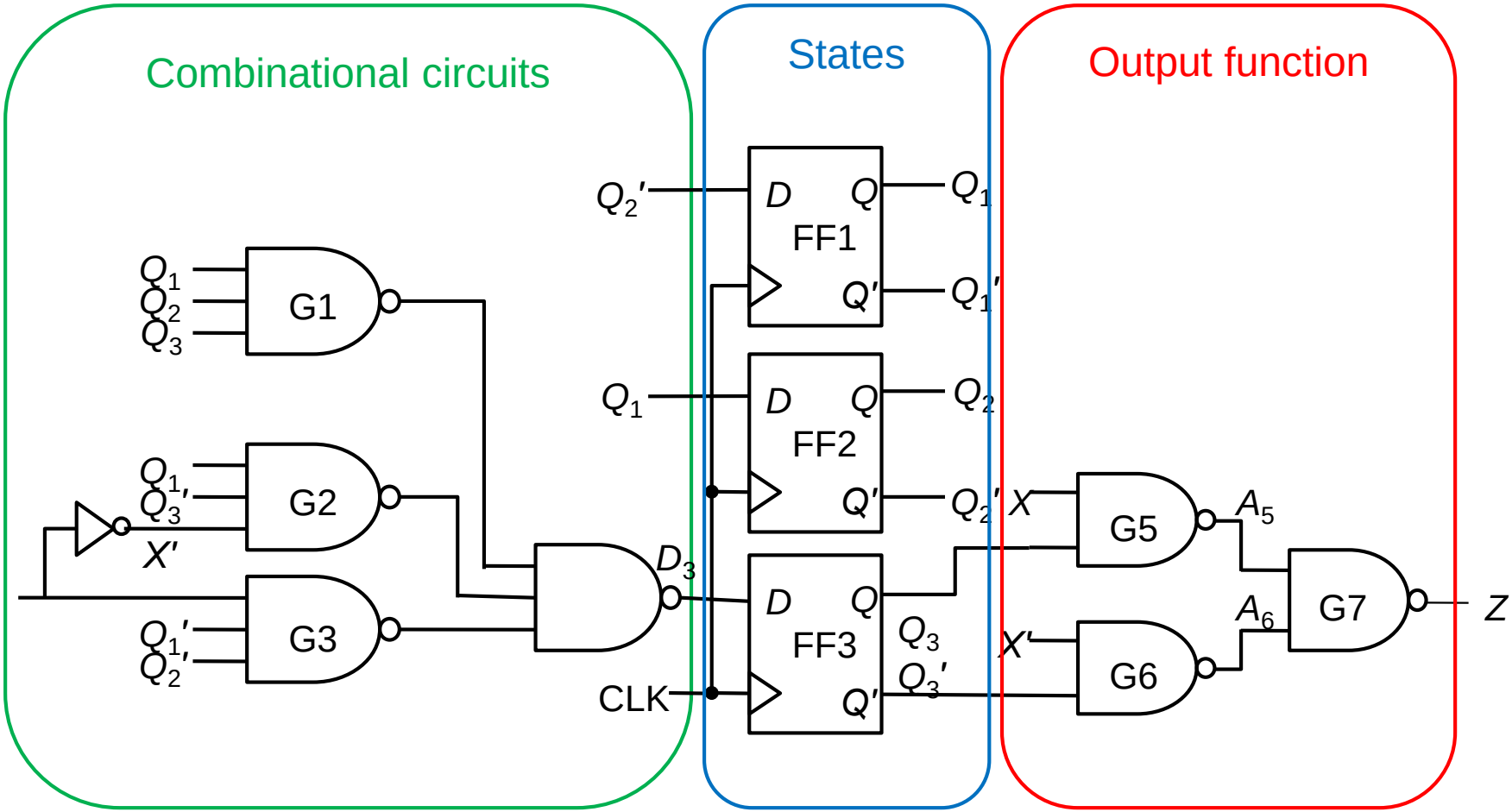
- **Realize circuit**



Sequential CKTs Using ROMs and PLAs

Combinational circuits	States	Output function
ROM/PLA	FFs	ROM/PLA

Sequential Circuit Design with ROMs/PLAs

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- **BCD to excess-3 code converter**
  - State table

Present state	Next state $X=0$	Next state $X=1$	Present Output (Z) $X=0$	Present Output (Z) $X=1$
A	*B*	*C*	1	0
B	*D*	*E*	1	0
C	*E*	*E*	0	1
D	*H*	*H*	0	1
E	*H*	*M*	1	0
H	*A*	*A*	0	1
M	*A*	-	1	-

  - Transition table

		$Q_1^+Q_2^+Q_3^+$		Z	
	$Q_1Q_2Q_3$	$X=0$	$X=1$	$X=0$	$X=1$
A	0 0 0	0 0 1	0 1 0	1	0
B	0 0 1	0 1 1	1 0 0	1	0
C	0 1 0	1 0 0	1 0 0	0	1
D	0 1 1	1 0 1	1 0 1	0	1
E	1 0 0	1 0 1	1 1 0	1	0
H	1 0 1	0 0 0	0 0 0	0	1
M	1 1 0	0 0 0	x x x	1	x
-	1 1 1	x x x	x x x	x	x

Using a ROM and D FFs? (1/2)

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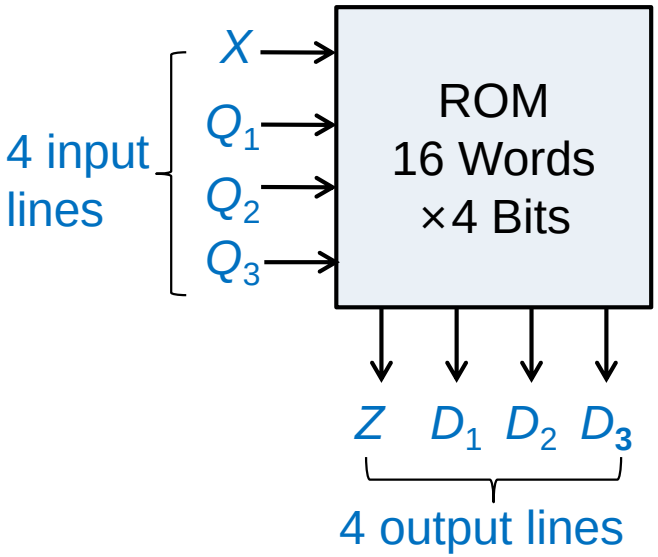
- **Realize it using a ROM and D FFs**
  - Realize D FF input eq. and output eq. by a ROM



X	Q_1	Q_2	Q_3	Z	D_1	D_2	D_3
0	0	0	0	1	0	0	1
0	0	0	1	1	0	1	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	1	1	0	1
0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	x	x	x	x
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	1	0	0	0
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Using a ROM and D FFs? (2/2)

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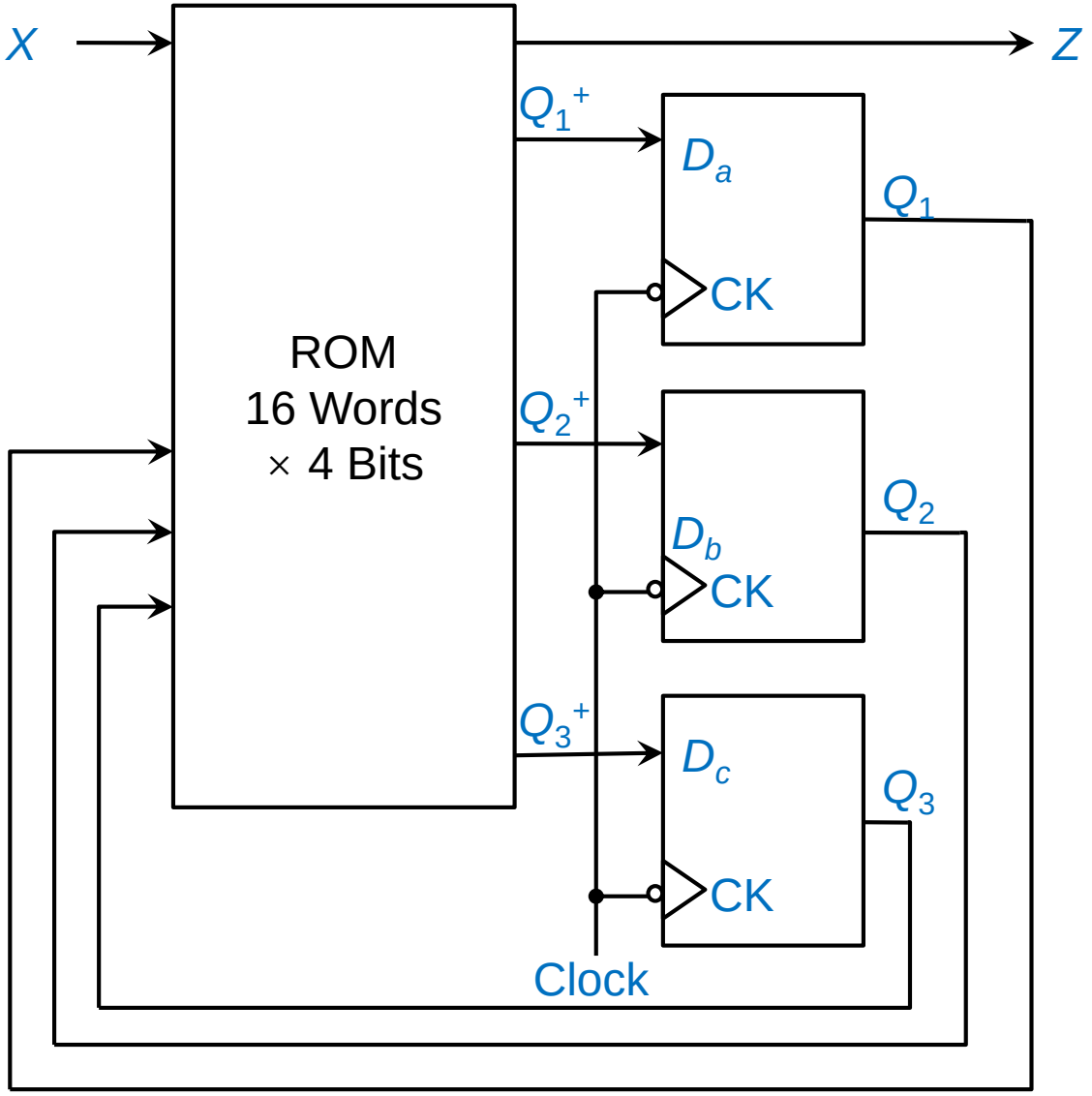

Using a PLA and D FFs? (1/2)

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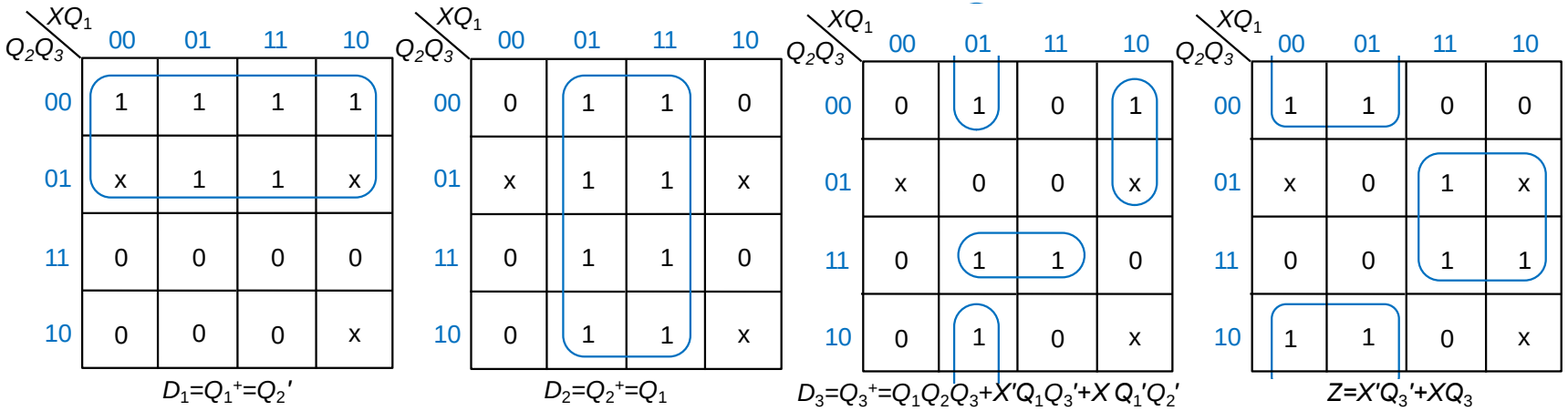
- **Realize it using a PLA and D FFs**
  - Realize D FF input eq. by a PLA



$D_1=Q_1^+=Q_2'$

$D_2=Q_2^+=Q_1$

$D_3=Q_3^+=Q_1Q_2Q_3+X'Q_1Q_3'+XQ_1'Q_2'$

$Z=X'Q_3'+XQ_3$

Using a PLA and D FFs? (2/2)

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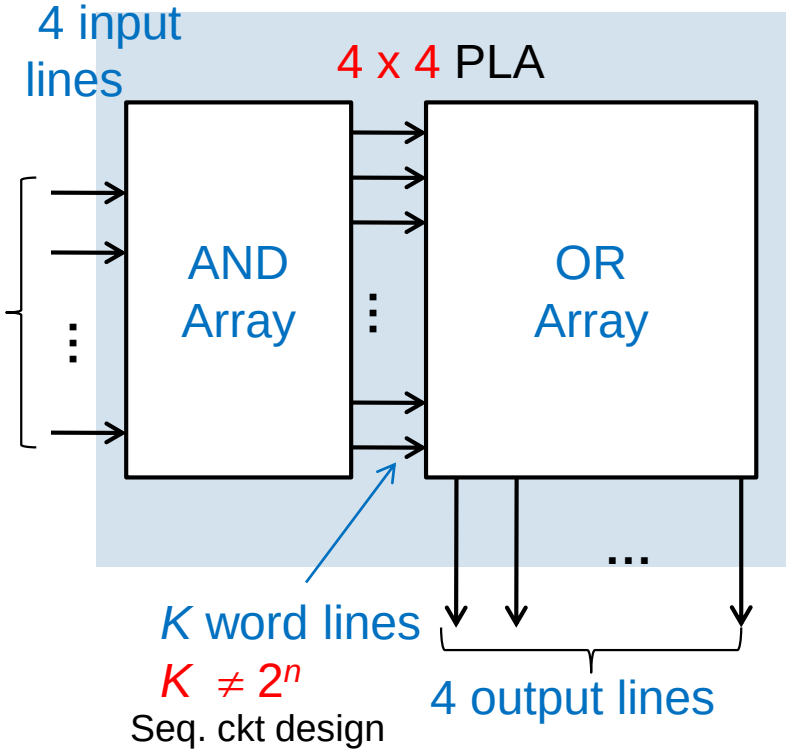
$D_1=Q_1^+=Q_2'$

$D_2=Q_2^+=Q_1$

$D_3=Q_3^+=Q_1Q_2Q_3+X'Q_1Q_3'+XQ_1'Q_2'$

$Z=X'Q_3'+XQ_3$



Product term	Inputs X	Q_1	Q_2	Q_3	Outputs Z	D_1	D_2	D_3
Q_2'	–	–	0	–	0	1	0	0
Q_1	–	1	–	–	0	0	1	0
$Q_1Q_2Q_3$	–	1	1	1	0	0	0	1
$X'Q_1Q_3'$	0	1	–	0	0	0	0	1
$XQ_1'Q_2'$	1	0	0	–	0	0	0	1
$X'Q_3'$	0	–	–	0	1	0	0	0
XQ_3	1	–	–	1	1	0	0	0

AND plane

OR plane

Design of Iterative Circuits

A comparator

Iterative Circuits

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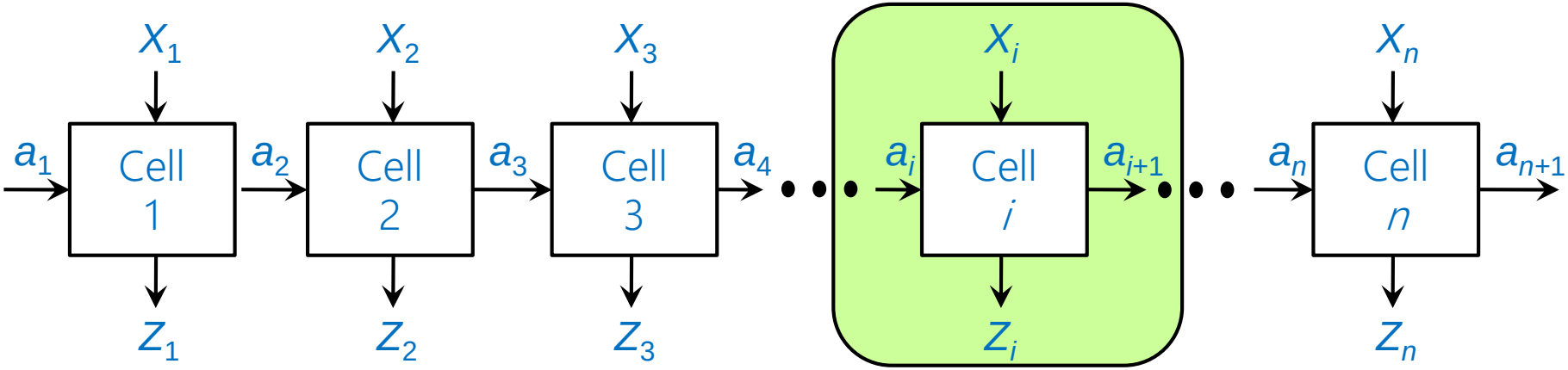
- **An iterative circuit consists of a number of identical cells interconnected by a regular structure**
  - The design is very similar to that of a sequential circuit
  - The simplest form: a unilateral iterative circuit
    - A linear array of combinational cells
    - Signals between cells traveling in only one direction
    - Parallel-input parallel-output



Design of a Sequential Comparator (1/5)

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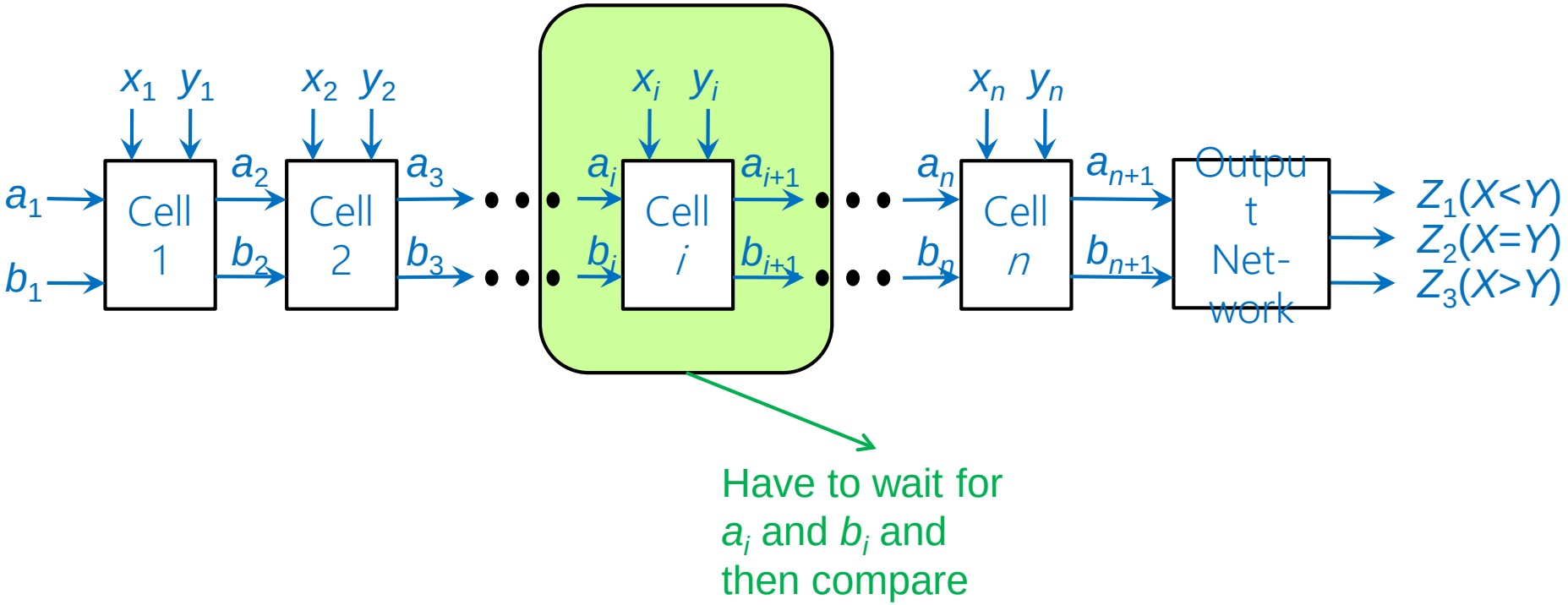
- **Form of iterative circuit for comparing binary numbers**
  - $X = x_1x_2x_3\ldots x_n$
  - $Y = y_1y_2y_3\ldots y_n$

time $t_1\ t_2\ t_3\ \ldots\ t_n$

x_1, y_1: MSB (most significant bit)



Design of a Sequential Comparator (2/5)

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- **State table**

S_i	S_{i+1} x_iy_i = 00	01	11	10	$Z_1Z_2Z_3$
$X=Y$ S_0	S_0	S_2	S_0	S_1	0 1 0
$X>Y$ S_1	S_1	S_1	S_1	S_1	0 0 1
$X<Y$ S_2	S_2	S_2	S_2	S_2	1 0 0

$Z_1(X<Y)$
$Z_2(X=Y)$
$Z_3(X>Y)$

- **Transition table**
  - State assignment: S_0:00 S_1:01 S_2:10

a_ib_i	$a_{i+1}b_{i+1}$ x_iy_i = 00	01	11	10	$Z_1Z_2Z_3$
$X=Y$ 00	00	10	00	01	0 1 0
$X>Y$ 01	01	01	01	01	0 0 1
$X<Y$ 10	10	10	10	10	1 0 0

Design of a Sequential Comparator (3/5)

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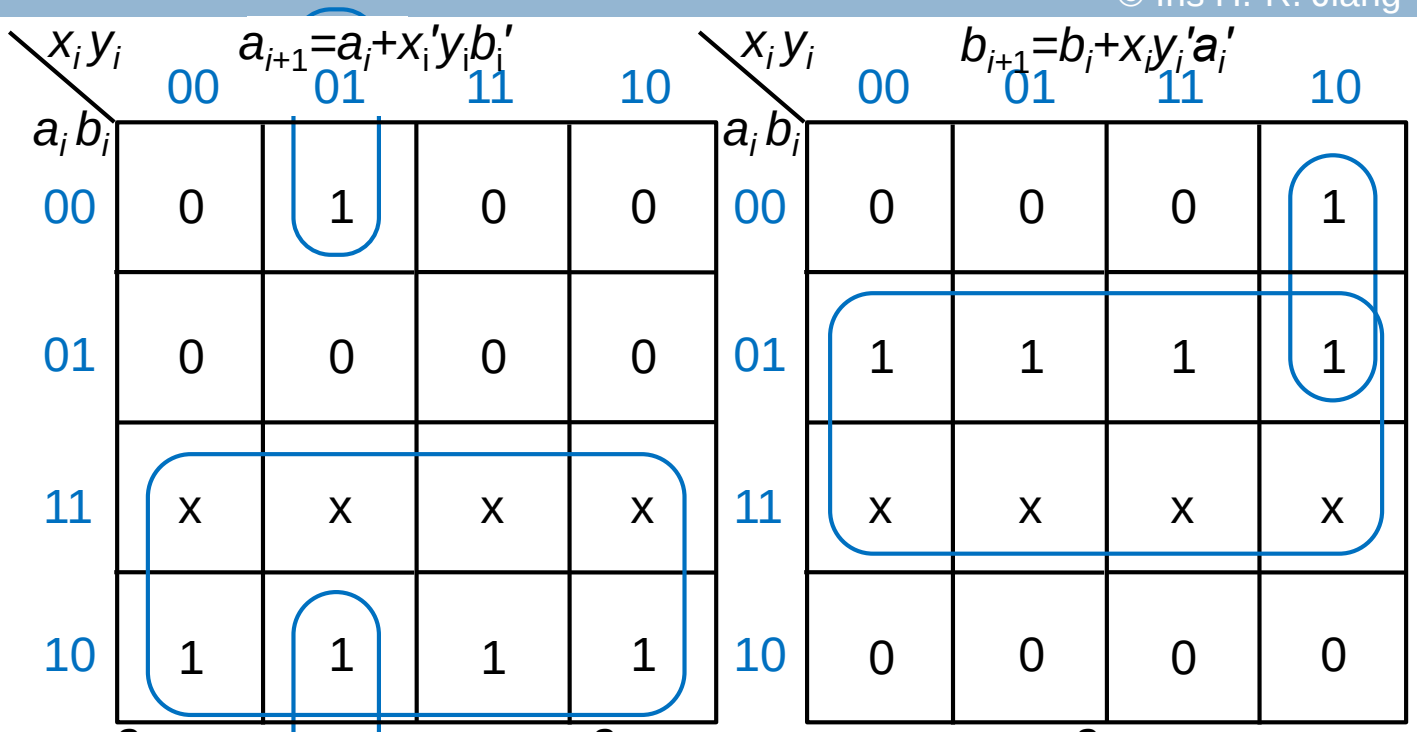
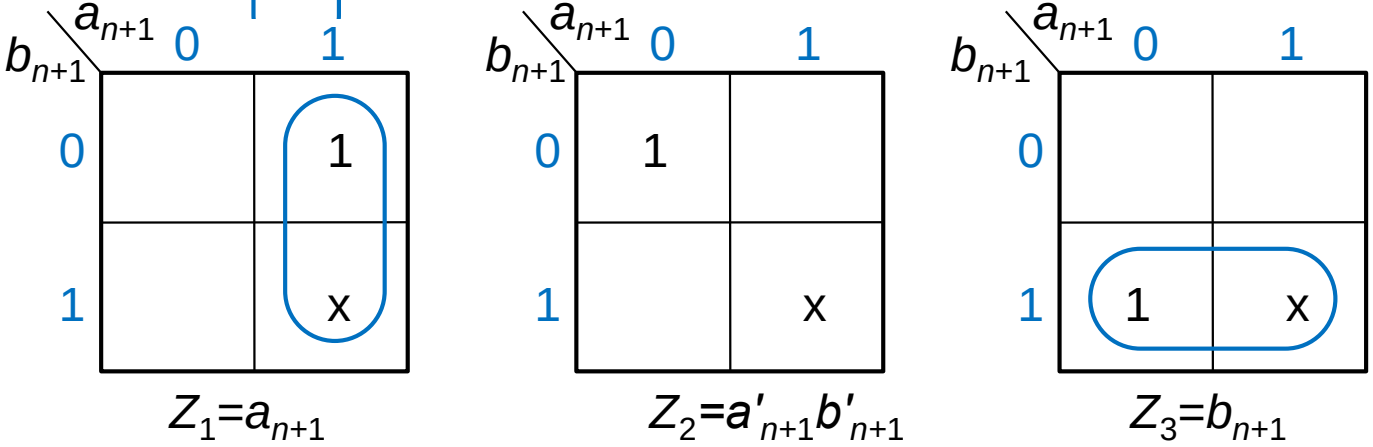
- **Typical cell**



- **Output**



Design of a Sequential Comparator (4/5)

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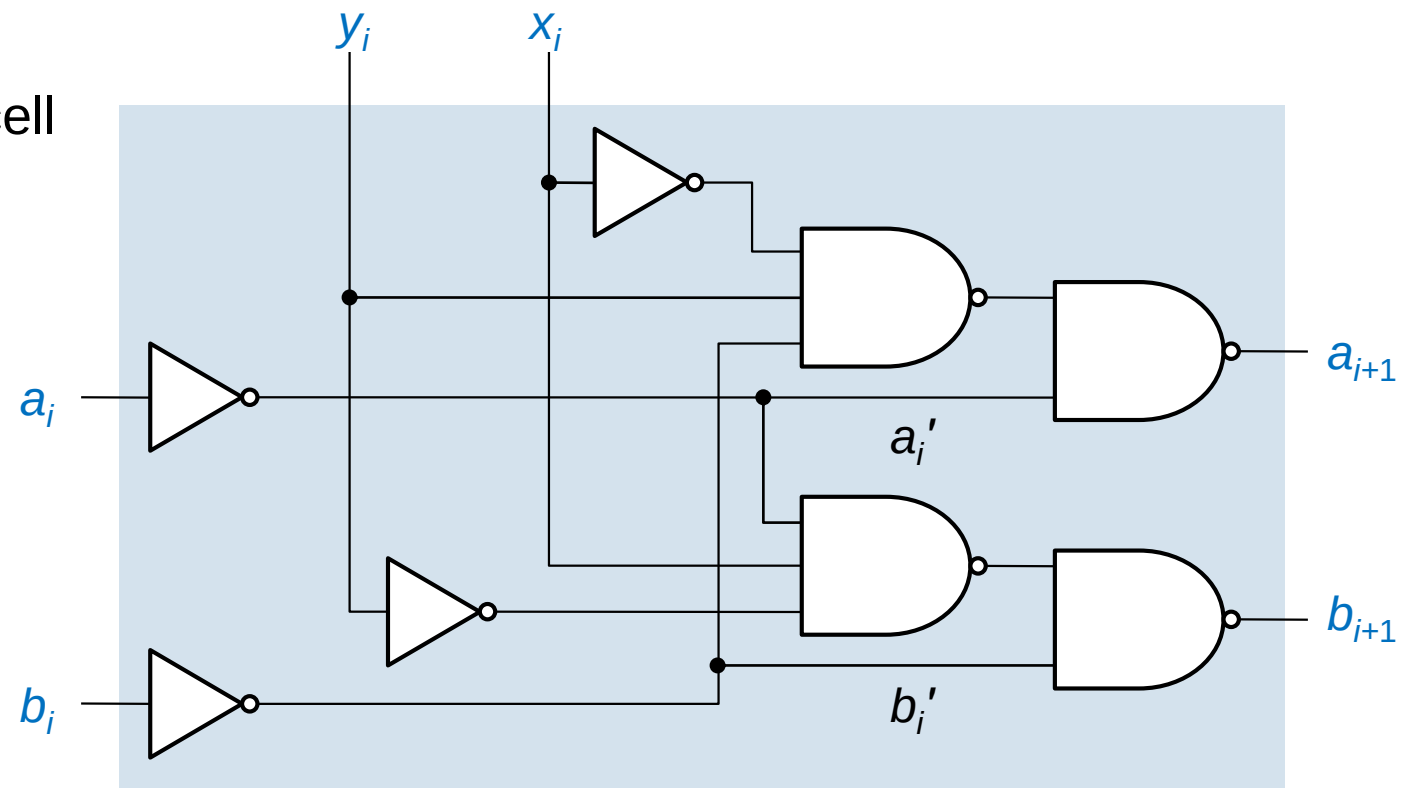
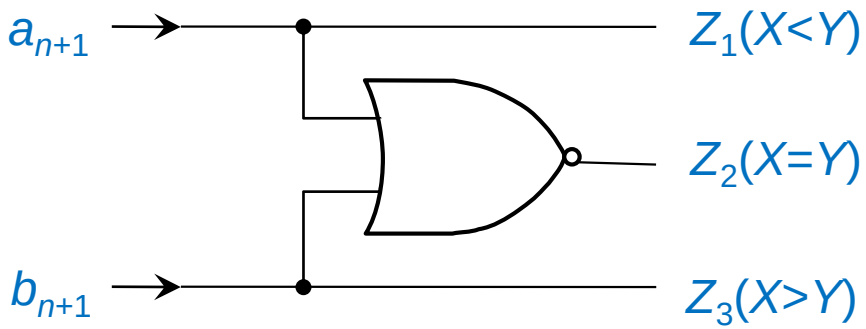
- **Circuit**
  - Typical cell



  - Output ckt



Design of a Sequential Comparator (5/5)

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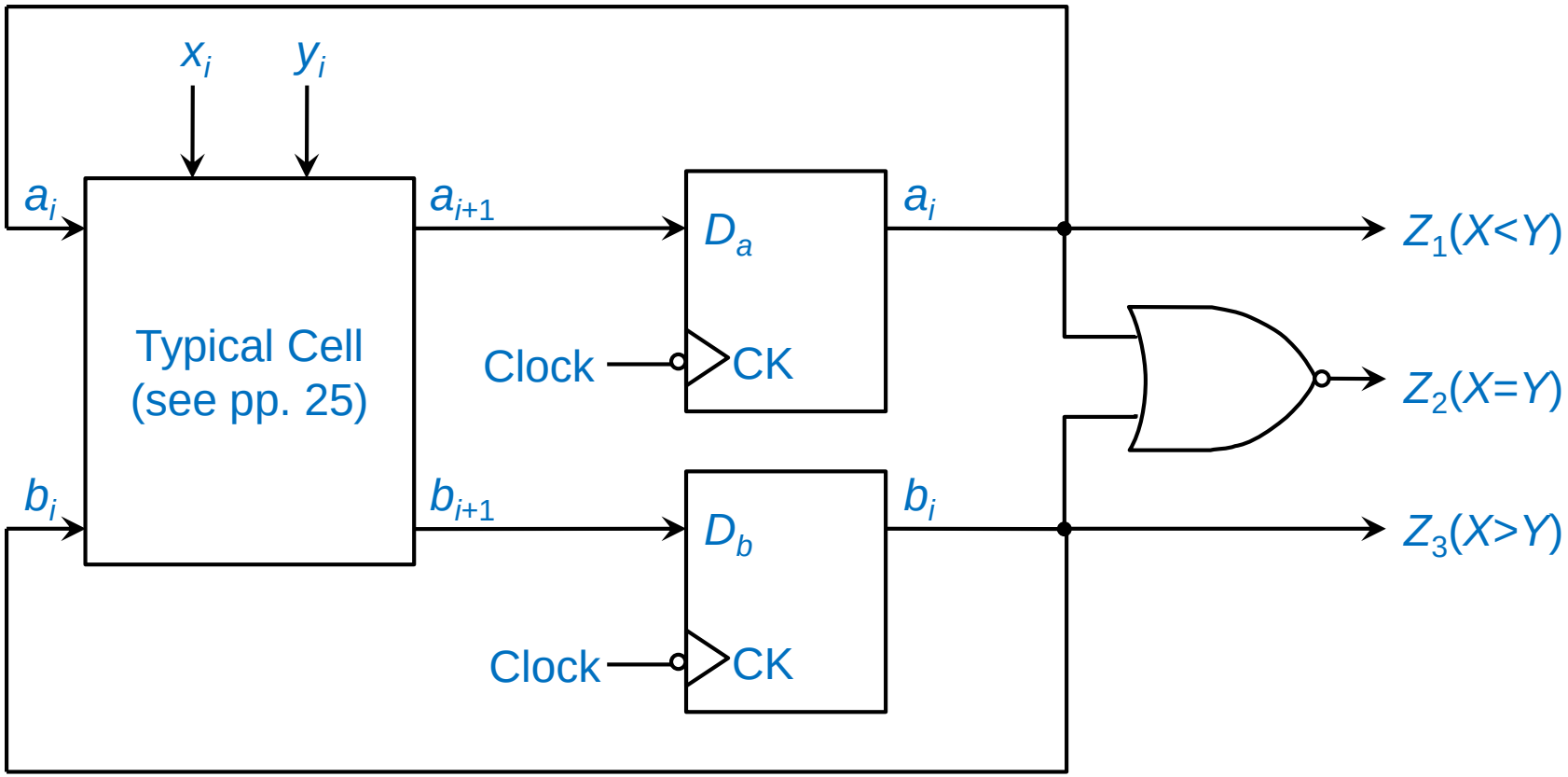
- **Complete circuit**
  - $X = x_1x_2x_3\ldots x_n$
  - $Y = y_1y_2y_3\ldots y_n$

time $t_1\ t_2\ t_3\ \ldots\ t_n$

x_1, y_1: MSB (most significant bit)
x_n, y_n: LSB (least significant bit)



Summary: Designing a Sequential Circuit

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