UNIT 8
COMBINATIONAL CIRCUIT DESIGN AND SIMULATION

Fall 2021

Combinational Circuit Design & Simulation

- **Contents**
  - Review of combinational circuit design
  - Design of circuits with limited gate fan-in
  - Gate delay and timing diagrams
  - Hazards in combinational logic
  - Simulation and testing of logic circuits
- **Reading**
  - Unit 8

Review of Combinational Circuit Design

- **Generic combinational circuit design steps:**
  1. Specify the switching function(s)
     - A truth table
     - Algebraic equations
  2. Derive simplified algebraic expression(s)
     - Karnaugh maps
     - Algebraic simplification (large # of variables, small # of terms)
  3. Manipulate into the proper form
     - Apply algebraic simplification with considering the gate types used in circuit implementation
- **Minimum SOP (POS) $\Rightarrow$ minimum two-level circuits**
  - Start from min SOP $\equiv$ AND-OR $\Rightarrow$ NAND-NAND/OR-NAND/NOR-OR
  - Start from min POS $\equiv$ OR-AND $\Rightarrow$ NOR-NOR/AND-NOR/NAND-AND
- **The # of level = the max # of cascaded gates between I/Os**
  - Change level by factoring or multiplying out
  - $\Rightarrow$ Change # of gates or gate inputs
- **Design a multi-level multi-output ckt from a ckt of AND & OR gates**

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Limited Gate Fan-in

For a gate, fan-in = # of inputs
For a circuit, fan-in = max # of inputs on each gate

Example 1

□ **Realize $f(a, b, c, d) = \Sigma\, m(0, 3, 4, 5, 8, 9, 10, 14, 15)$ using 3-input NOR gates**
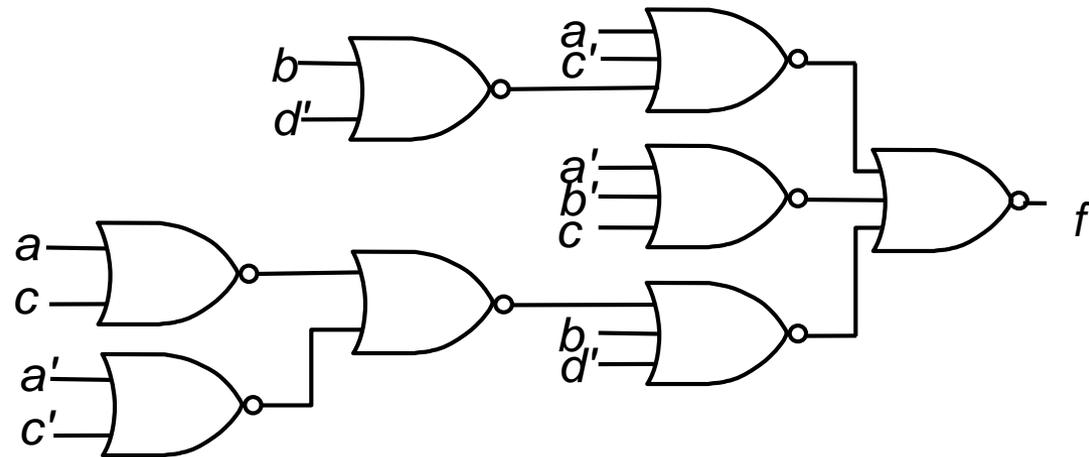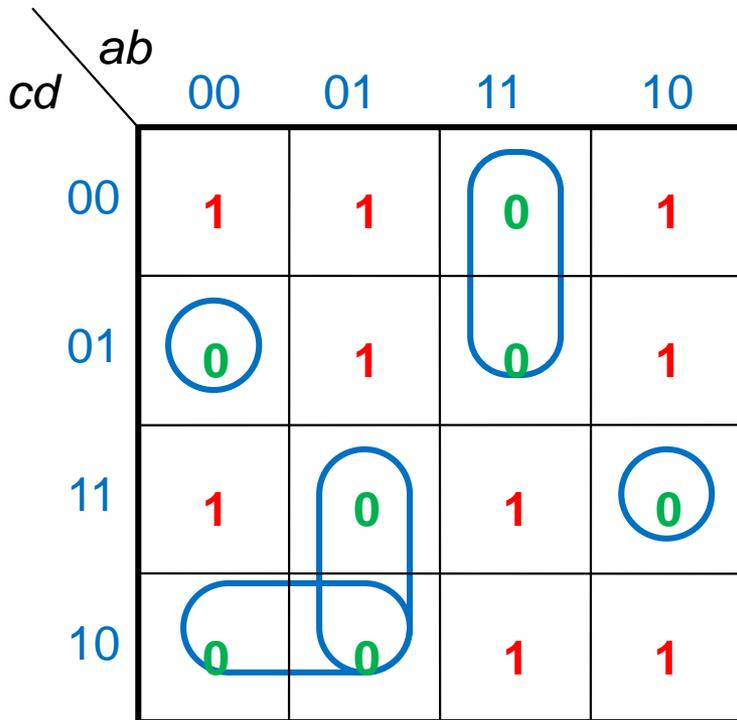
$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$

$\Rightarrow$ two-level circuit:

2 4-input AND (X) $\Rightarrow$ factoring
3 3-input AND (O)
1 5-input OR   (X) $\Rightarrow$ sum of 3 items

$\Rightarrow f' = b'd(a'c' + ac) + a'c(b + d') + abc'$

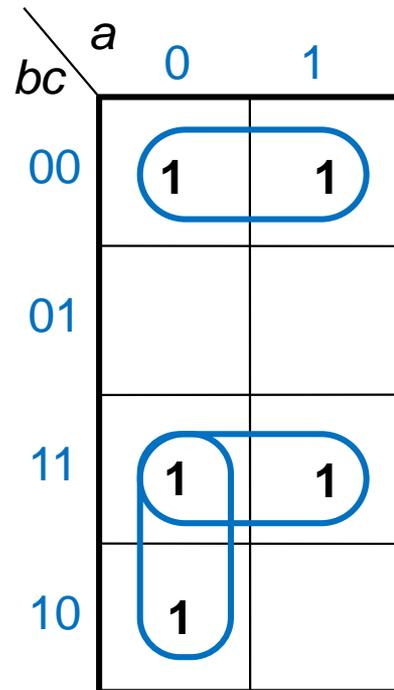$\Rightarrow f = [b + d' + (a + c)(a' + c')][a + c' + b'd][a' + b' + c]$

f

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Example 2 (1/2)

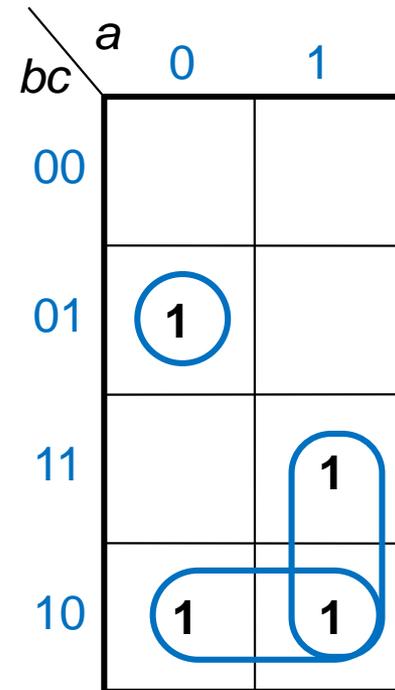□ **Realize the functions using only 2-input NAND gates and inverters**
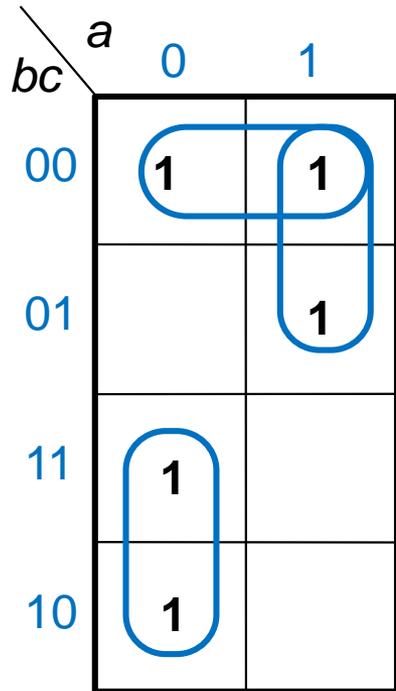
$f_1 = \Sigma\, m(0,2,3,4,5)$

$f_1 = b'c' + ab' + a'b$
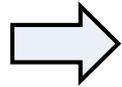
$f_2 = \Sigma\, m(0,2,3,4,7)$

$f_2 = b'c' + bc + a'b$
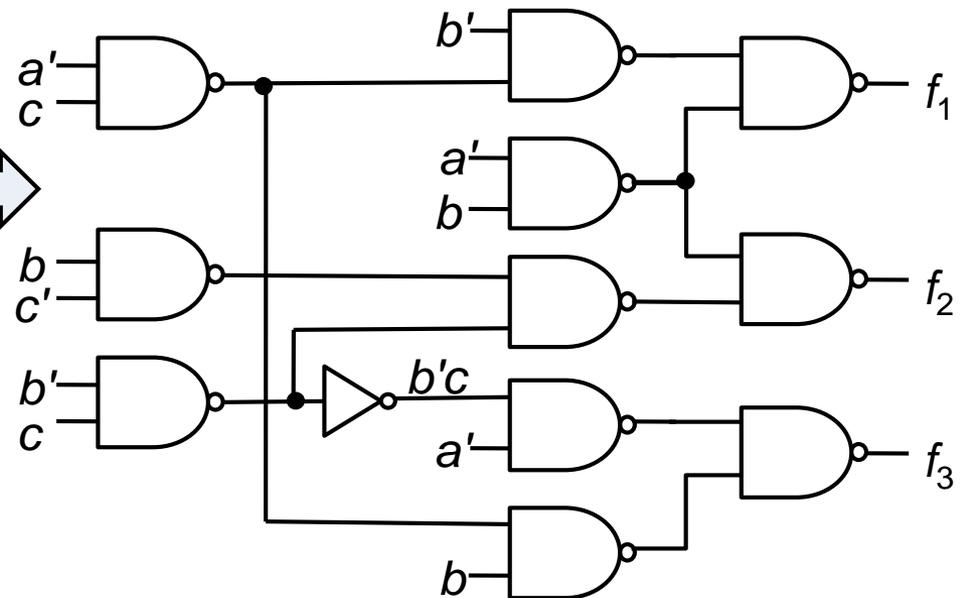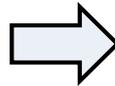
$f_3 = \Sigma\, m(1,2,6,7)$

$f_3 = a'b'c + ab + bc'$

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Example 2 (2/2)

$f_1 = b'c' + ab' + a'b$
$f_2 = b'c' + bc + a'b$
$f_3 = a'b'c + ab + bc'$

$\Rightarrow$

$f_1 = b'(a + c') + a'b$
$f_2 = b'c' + b(a' + c)$ or $f_2 = (b' + c)(b + c') + a'b$
$f_3 = a'(b + c')' + b(a + c')$

$a'b'c = a'(b'c) = a'(b + c')'$

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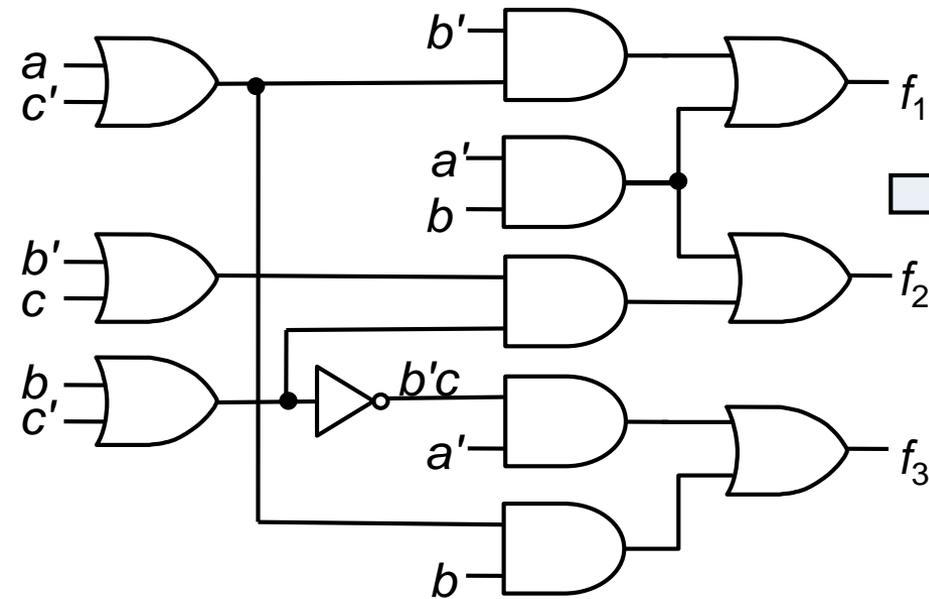
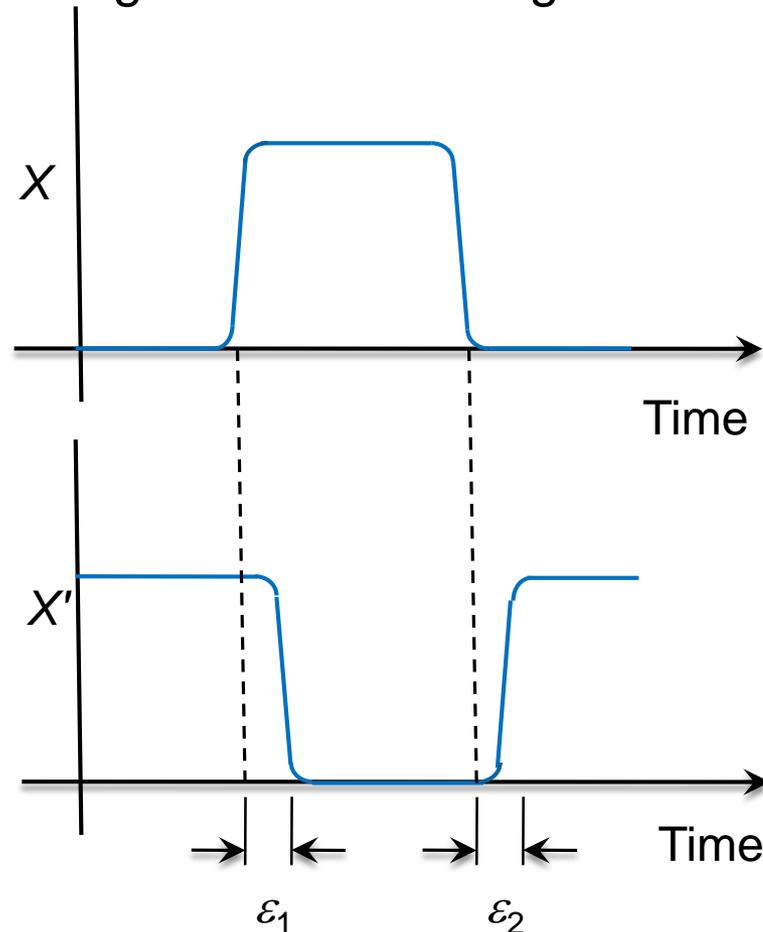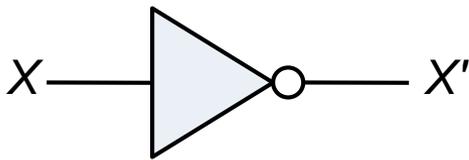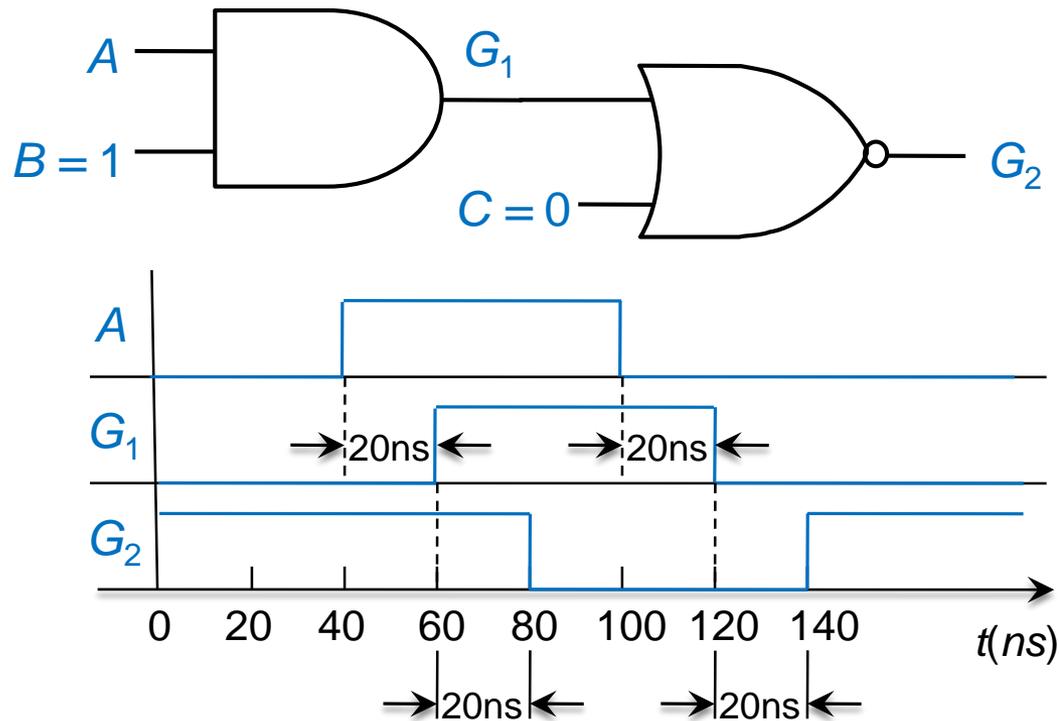**8** Gate Delays and Timing Diagrams

Gate Delay

- **Propagation delay: when the input to a logic gate is changed, the output takes some time to change value**
  - Usually different for input rising $0 \to 1$ and falling $1 \to 0$
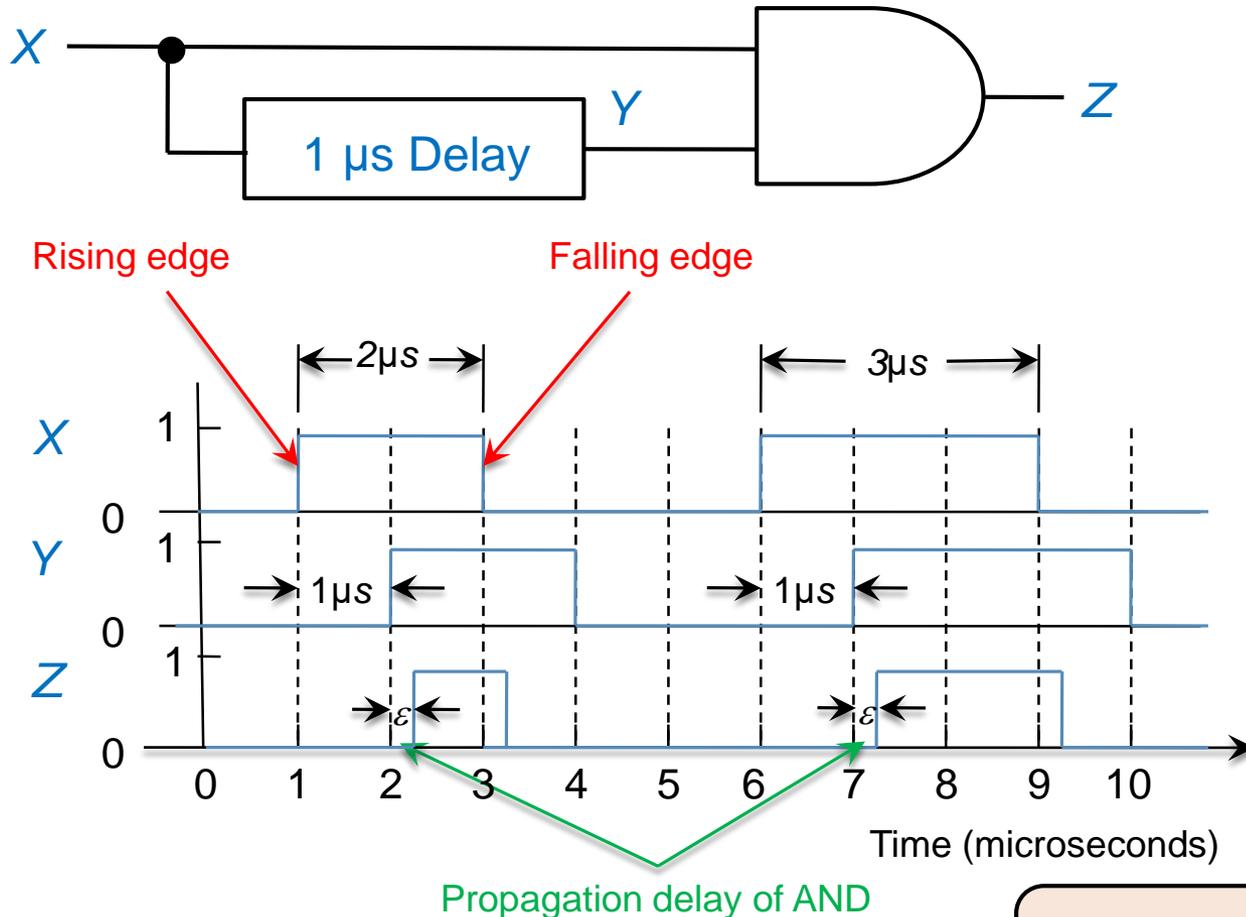
A few ns
(nanosecond = 10^{-9} sec)

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Sample Timing Diagram (1/2)

□ **e.g., assume each gate has a propagation delay of 20 ns**

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Sample Timing Diagram (2/2)

□ **e.g., a circuit with a delay element**

Rising edge

Falling edge

Propagation delay of AND

μs
(microsecond = 10^{-6} sec)

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12 Hazards

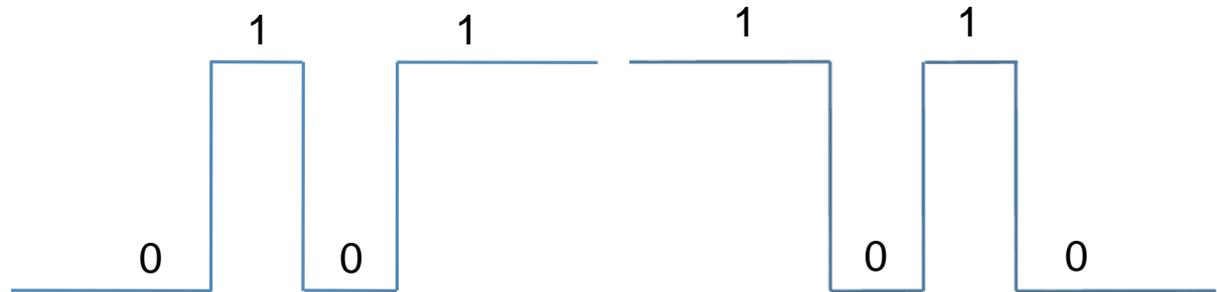Combinational circuit design & simulation

Hazards

□ **Hazard: unwanted switching transients appearing at the output when the input to a combinational ckt changes**

   ◻ Static 1-/0-hazard: output momentarily goes to 0/1 when it should remain a constant 1/0
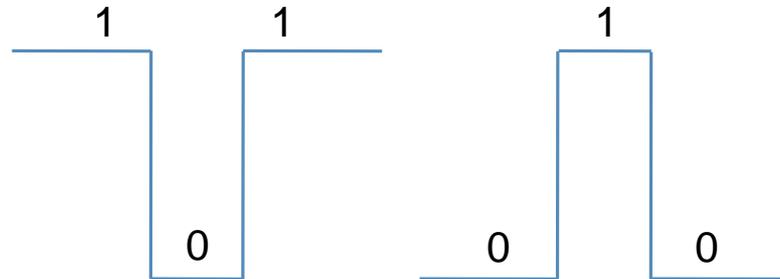
(a) Static 1-hazard   (b) Static 0-hazard

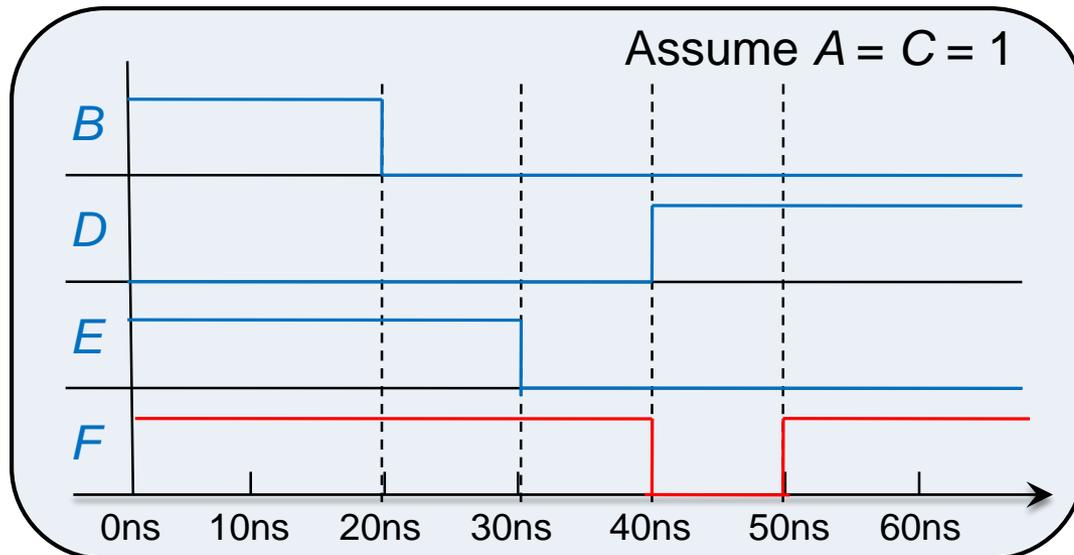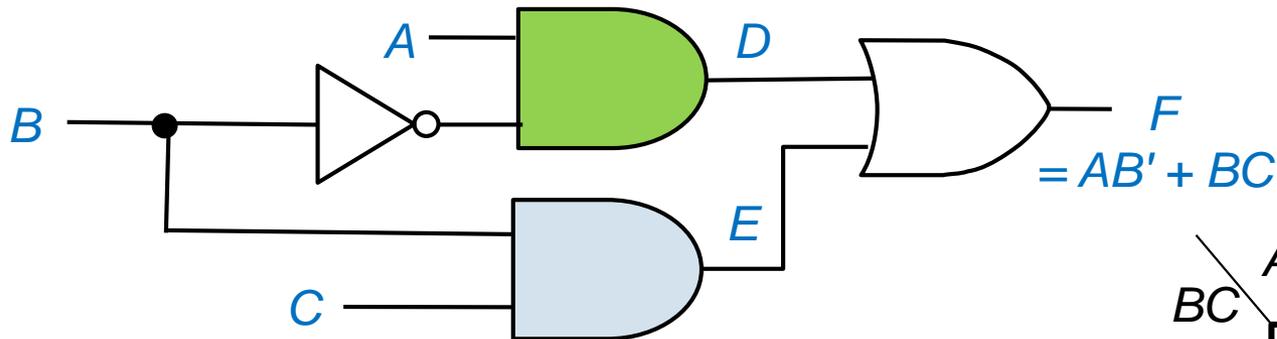   ◻ Dynamic hazard: output change 3 or more times when the output changes from 0 to 1 (1 to 0)

(c) Dynamic hazard

1-Hazards? When?

- e.g., assume each gate has a propagation delay of 10 ns
  If $A = C = 1$, **static-1 hazard** occurs when B changes from 1 to 0

$F = AB' + BC$

Assume $A = C = 1$

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1-Hazard Removal for 2-Level AND/OR Circuit

- □ **Q: When?**
- □ **A: In Karnaugh maps, if any two adjacent 1's are not covered by the same loop, a 1-hazard exists for the transition between the two 1's**

  Consider only one-input change!

- □ **Q: How to remove hazards?**
- □ **A: Add additional loops s.t. all adjacent 1's are covered by some loop**

$$F = AB' + BC + AC$$

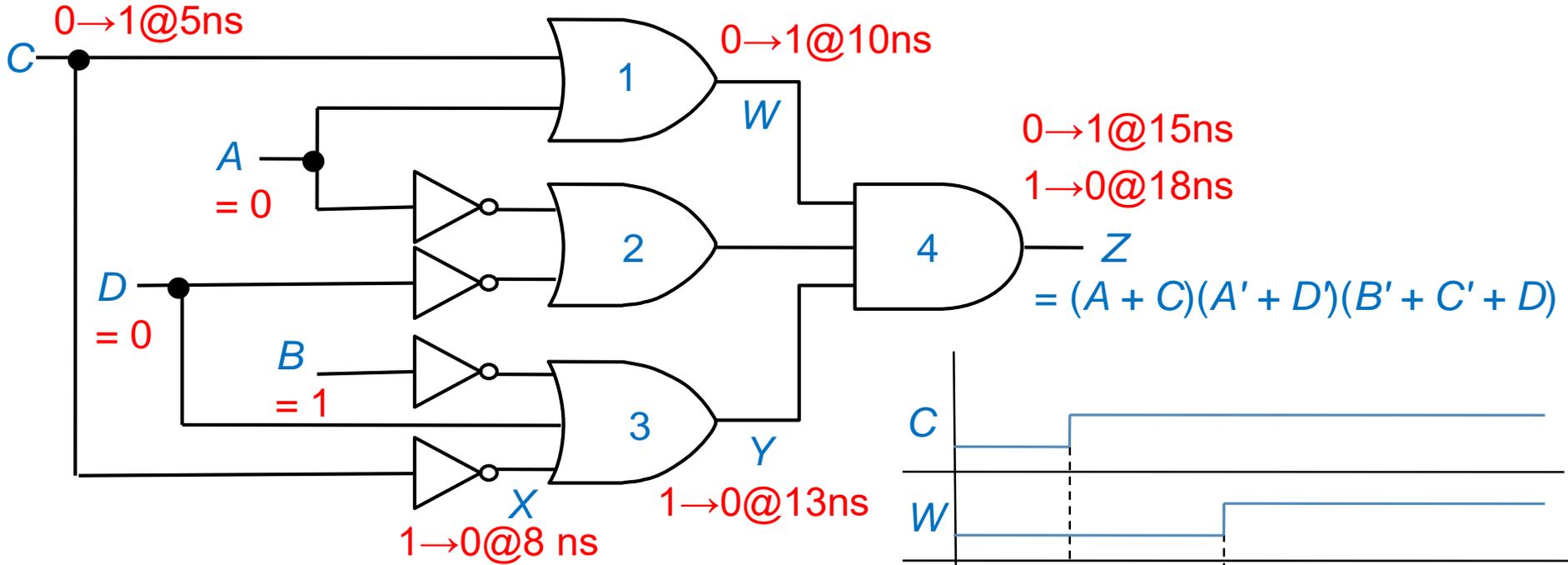| A	0	1
BC		
00	0	1
01	0	1
11	1	1
10	0	0

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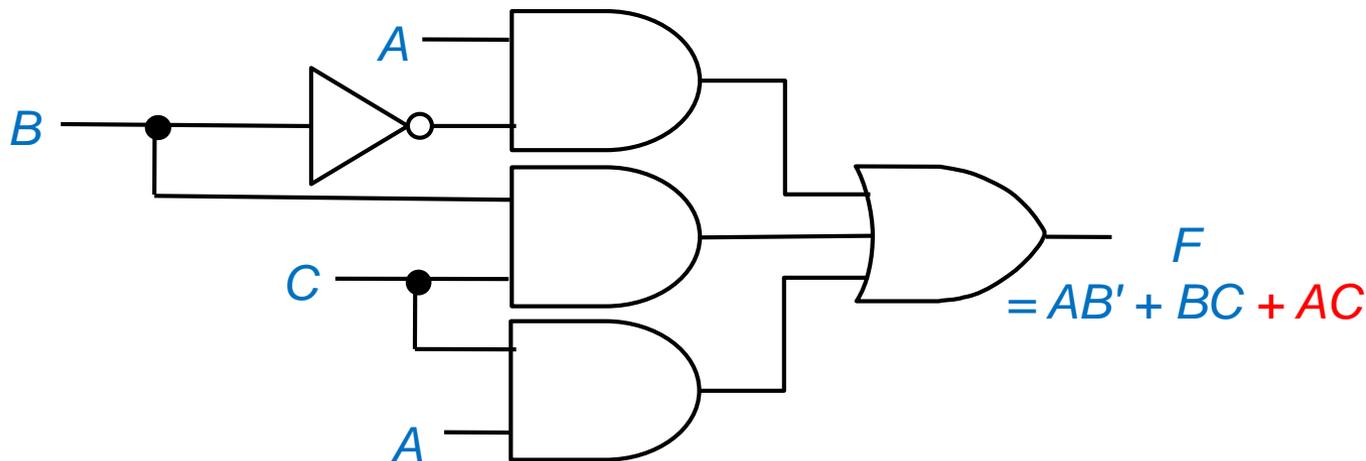
0-Hazards? When?

□ **e.g., consider $A = 0$, $B = 1$, $D = 0$, C changes from 0 to 1**

$0 \rightarrow 1@5\text{ns}$

$0 \rightarrow 1@10\text{ns}$

C

1

W

A
= 0

2

D
= 0

4

$0 \rightarrow 1@15\text{ns}$
$1 \rightarrow 0@18\text{ns}$

Z
$= (A + C)(A' + D')(B' + C' + D)$

B
= 1

3

Y

X

$1 \rightarrow 0@13\text{ns}$

$1 \rightarrow 0@8 \text{ ns}$

Propagation delay:
Inverter: 3 ns
AND/OR: 5 ns

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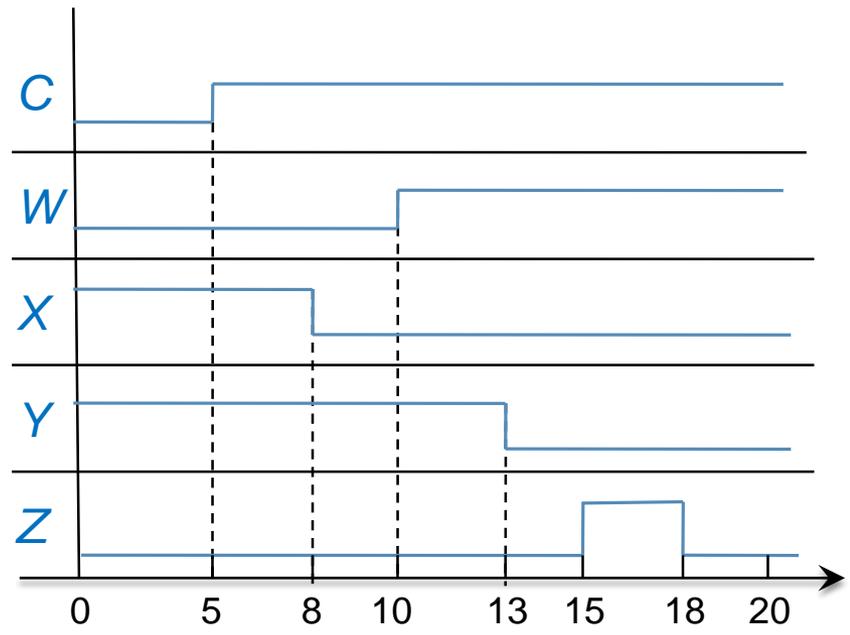
0-Hazard Removal for 2-Level AND/OR Circuit
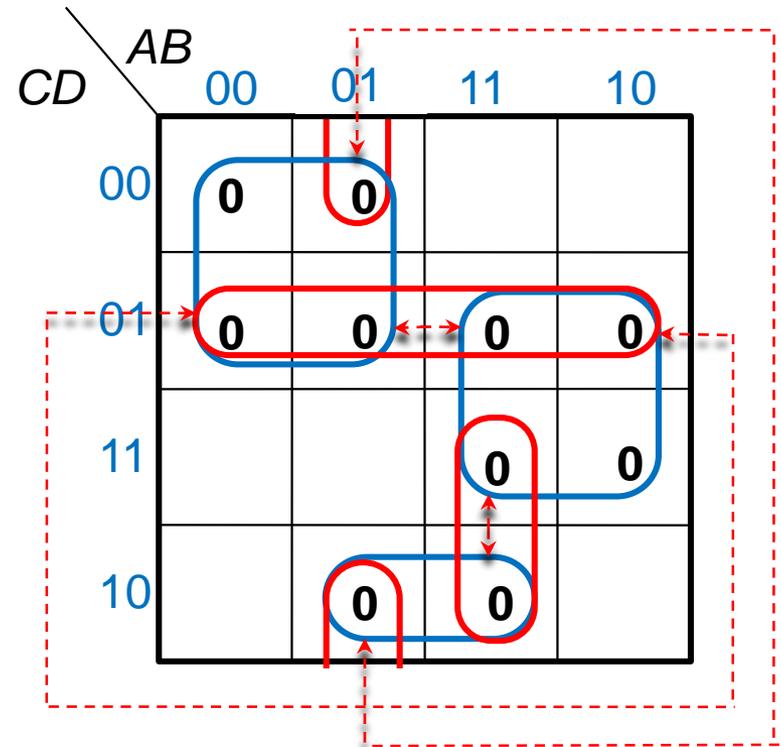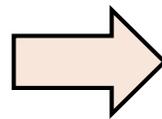
- **Similarly, add additional loops for adjacent 0's**

- **e.g,**

Consider only one-input change!
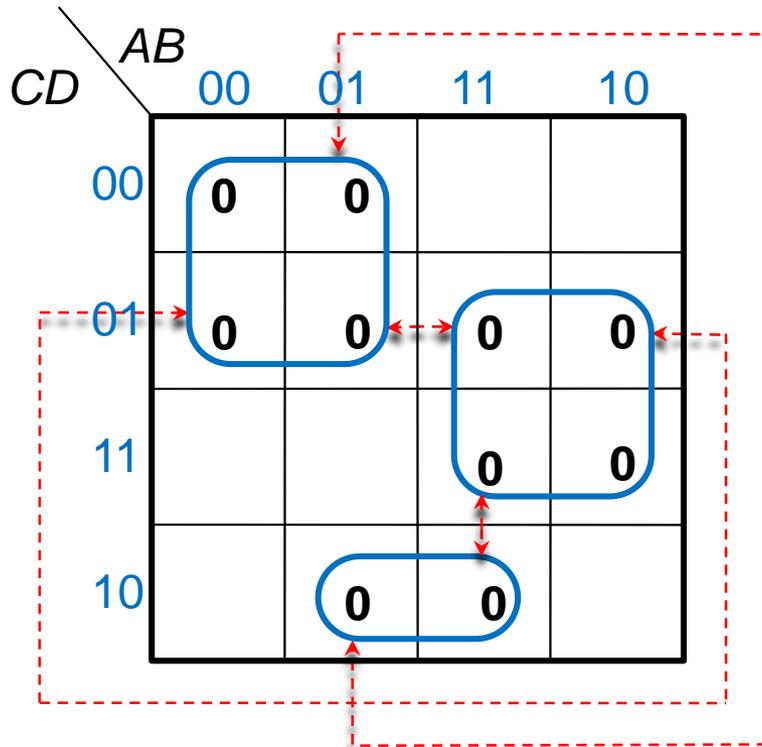
$Z = (A + C)(A' + D')(B' + C' + D)$

$Z = (A + C)(A' + D')(B' + C' + D)$
$(C + D')(A + B' + D)(A' + B' + C')$

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Simulation

- **Verify logic circuits by**
  - Actually building them
  - Simulating them on a computer
    - Computations are performed stage-by-stage from inputs
    - Evaluations are performed every time inputs change
- **4 logic values:** 0 (low), 1 (high), X (unknown), Z (high-Z/open ckt)

Probing gate outputs

missing gate input
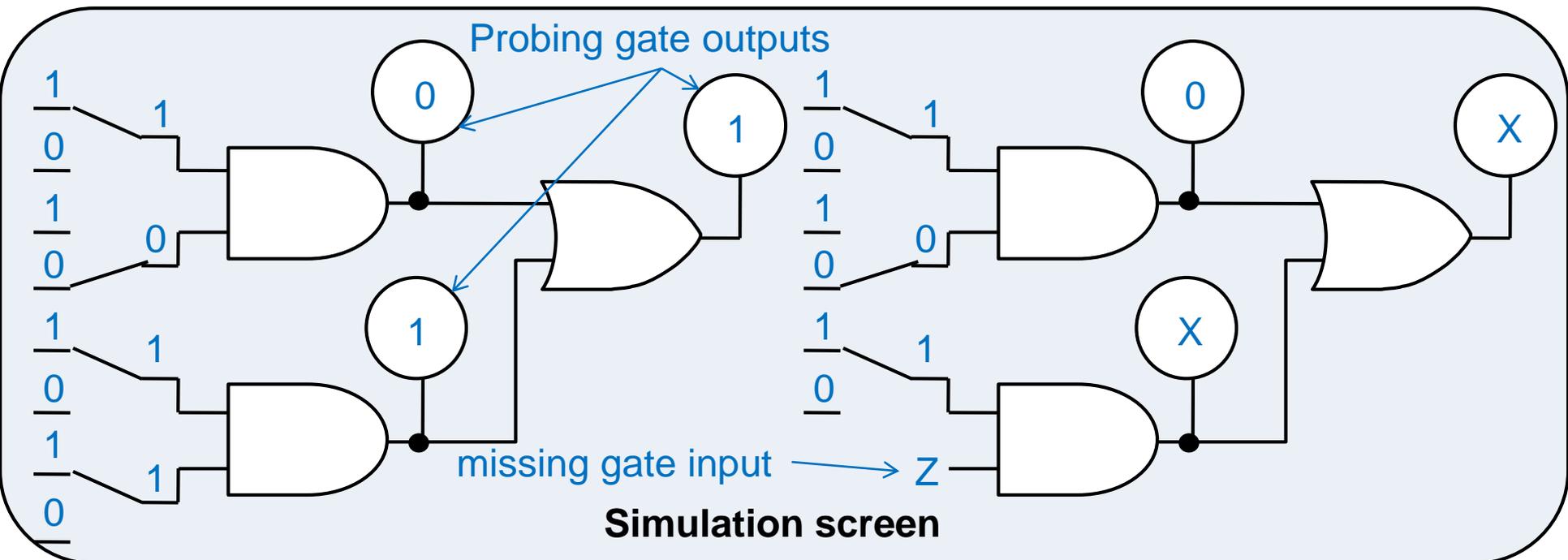
Simulation screen

4-Valued Logic Simulator

□ **AND and OR functions for 4-valued simulation**

●	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

□ **Possible errors in designs**
  ▫ In simulation
    - Incorrect design
    - Gates connected wrong
    - Wrong input signals to the circuits
  ▫ In real circuits
    - Defective gates
    - Defective connecting wires

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