Test-Pattern Compression & Test-Response Compaction

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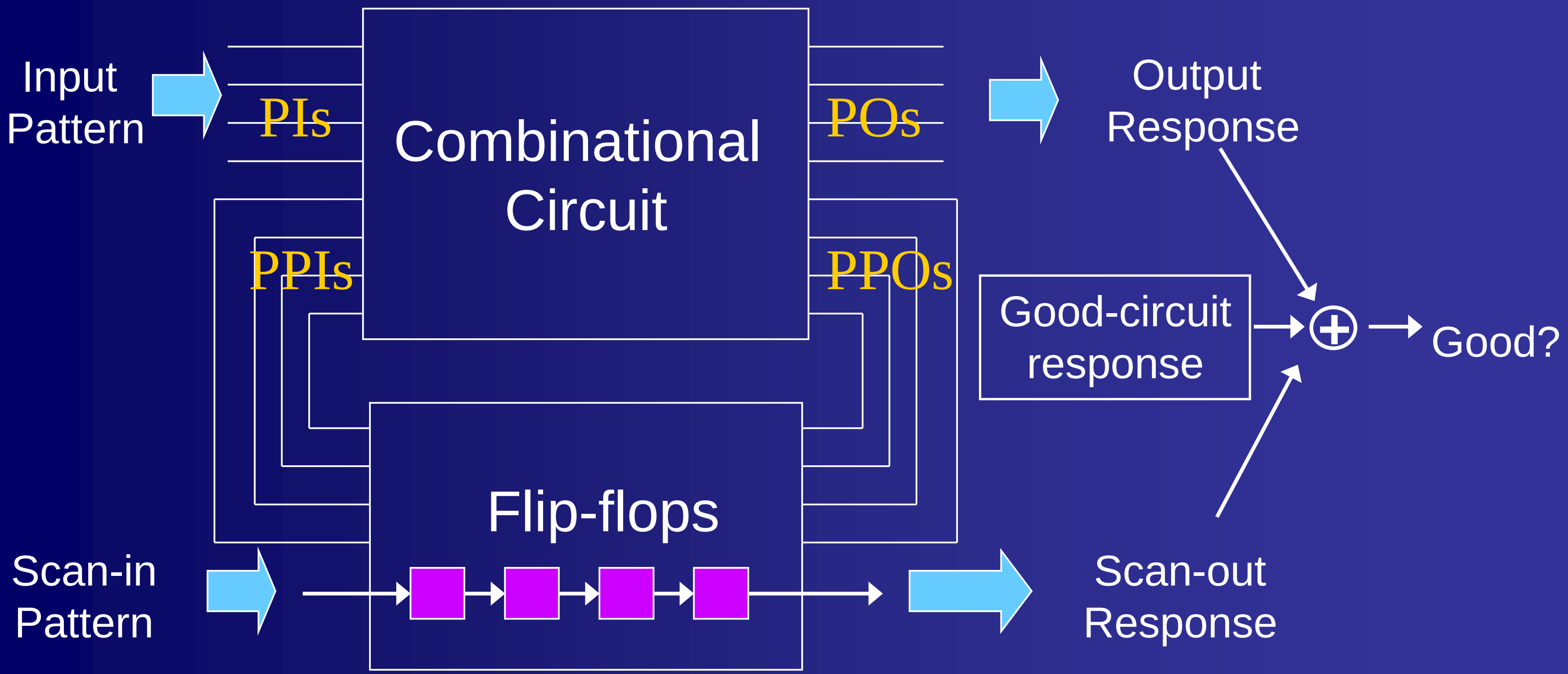
Outline

- Introduction to Scan-based Testing
- Input-Pattern Compression
  - Type of compressions
  - Compression schemes
  - Low-power decompression
- Output-Response Compaction
  - Time compactor (MISR)
  - Unknown-tolerant compaction schemes
  - Diagnosis with compactor
- Design Optimal Space Compactor
- Hybrid Compaction Scheme
- Conclusion

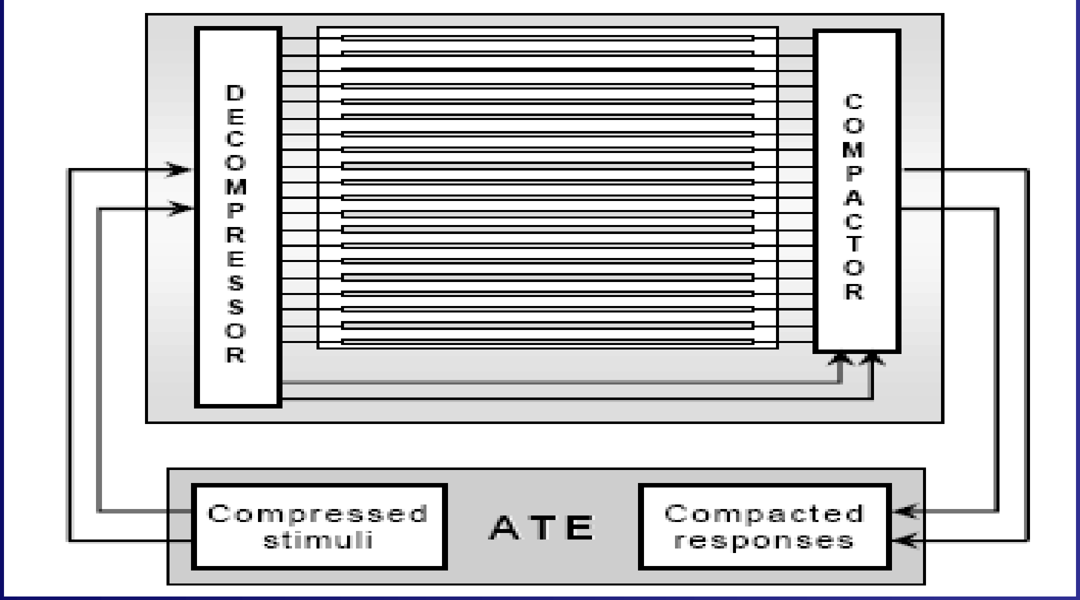
Scan-based Testing



- Advantage of scan
  - Better controllability and observability, lower ATPG complexity, higher fault coverage
- Disadvantage of scan
  - Long test-application time and large test-data volume

Input-Stimulus Compression & Output-Response Compaction

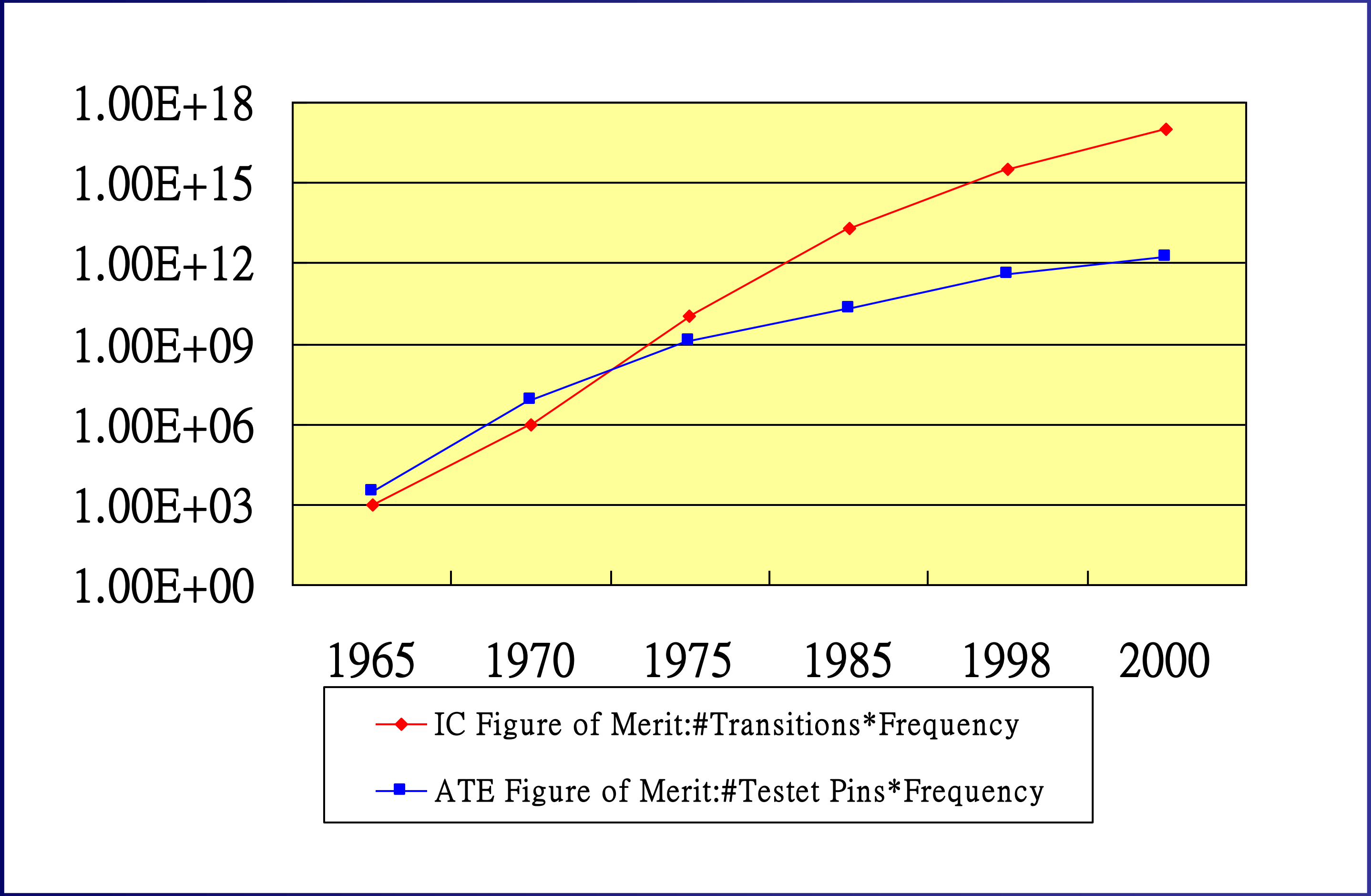
- Break a long scan chain into several short ones
- Still use limited ATE channels to supply test patterns and observe responses
- Save test-application time and test-data volume



IC/Tester Performance Comparison

		1965	1970	1975	1985	1998	2000
IC	No. of transistors	1	10	1000	10^6	10^7	10^8
	Frequency	1KHz	1MHz	10MHz	20MHz	300MHz	1GHz
	Figure of merit	1000	10^7	10^{10}	$2x10^{13}$	$3x10^{15}$	10^{17}
ATE	Tester pins	3	40	120	256	1024	2048
	Frequency	1KHz	200KHz	10MHz	80MHz	400MHz	800MHz
	Figure of merit	3000	$8x10^6$	$1.2x10^9$	$2x10^{10}$	$4X10^{11}$	$1.6X10^{12}$

IC/Tester Performance Comparison



Ideal Compression/Compaction Scheme

- No modification to functional logic
  - Such as test point insertion
- ATPG independent
  - Need not buy a new ATPG
- Pattern independent hardware
  - Changing test set need not changing hardware
- No coverage loss
  - Target fault model & un-modeled faults
- Small area overhead

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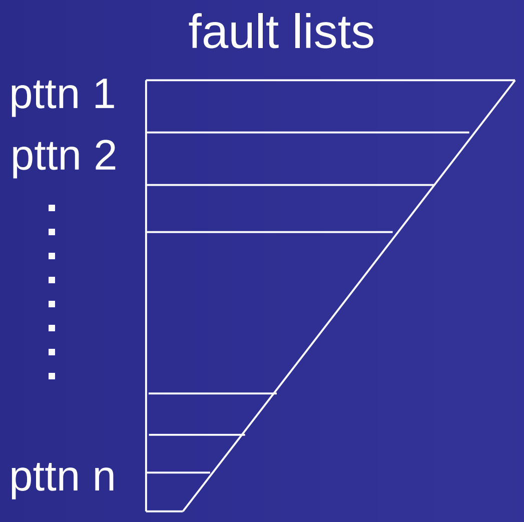
Pattern Compression vs. Compaction

- Compaction
  - less # of test vectors but still the same fault coverage
    - Compactable test cubes
    - Pattern re-ordering (due to fault dropping order)

Test cubes	Compacted
1XXXX0XX1 11XXXXX0X X1X0XXX0X	11X0X0X01
X011X1XXX 00XXXXX00	0011X1X00



- Compression
  - less # of bits per test vector

Vertical Compression vs. Horizontal Compression

- Vertical compression
  - Store one seed to supply multiple different patterns
  - # of seeds < # of deterministic patterns
  - # of applied patterns > # of deterministic patterns
  - Folding sequence [Liang ITC'01], XWork [NEC patent]
  - Mostly used in BIST architecture

- Horizontal compression
  - Length of a seed < length of a pattern

Input Compression Schemes

- Coding Strategy
  - Huffman coding, Run-length variable coding, Statistical coding
- LFSR Reseeding
  - Static reseeding, dynamic reseeding
- Broadcasting
  - Illinois Scan, reconfigurable switch
- Continuous-Flow Linear Expansion
  - SmartBist, Linear Network
- Mutation
  - Random access scan
- Low-power decompression scheme
  - low-power EDT

Run-Length Coding

- WWWWWWWWWWWWBWWWWWWWWWWWWBB
  BWWWWWWWWWWWWWWWWWWWWWWWWB
  WWWWWWWWWWWWWW

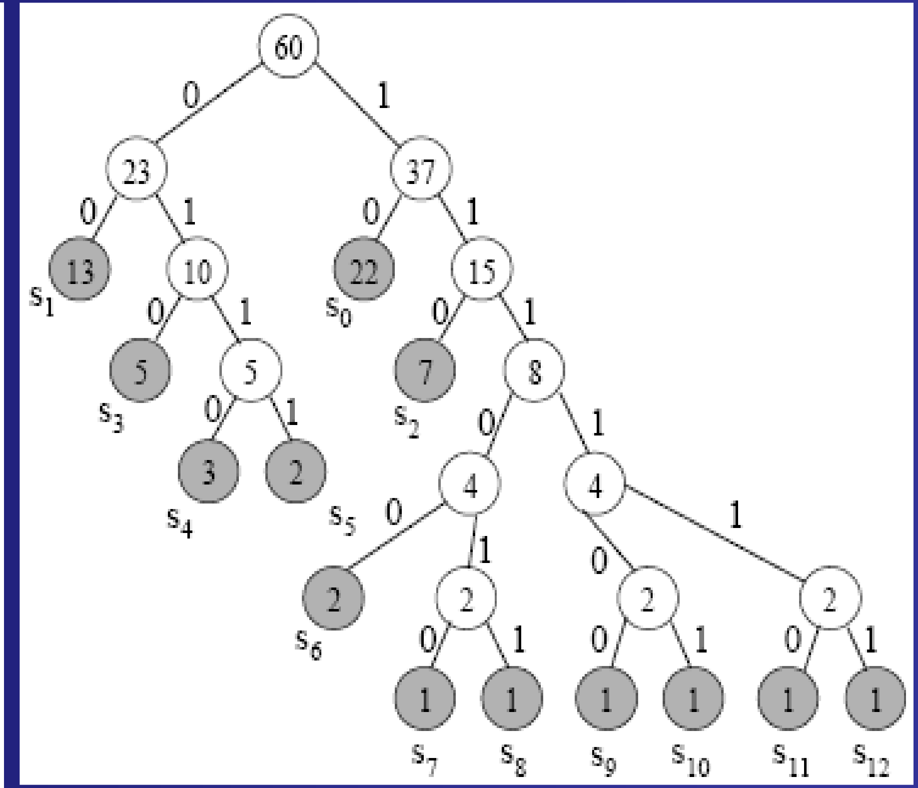
  ↓↓

- 12WB12W3B24WB14W
- Burrows-Wheeler transform can be used to maximize the run length

Statistical Coding

0010 0100 0010 0110 0000 0010 1011 0100 0010 0100 0110 0010
0010 0100 0010 0110 0000 0110 0010 0100 0110 0010 0010 0000
0010 0110 0010 0010 0010 0100 0100 0110 0010 0010 1000 0101
0001 0100 0010 0111 0010 0010 0111 0111 0100 0100 1000 0101
1100 0100 0100 0111 0010 0010 0111 1101 0010 0100 1111 0011

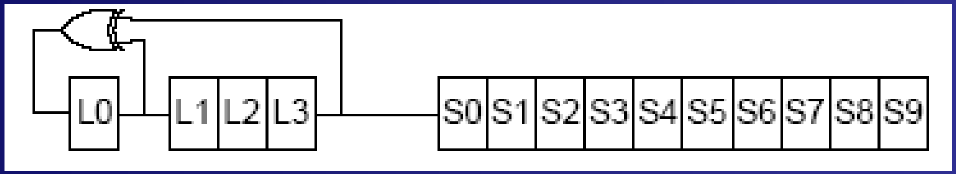
Sym.	Freq	Pat.	Huff. Code	Sel. Code
S_0	22	0010	10	10
S_1	13	0100	00	110
S_2	7	0110	110	111
S_3	5	0111	010	00111
S_4	3	0000	0110	00000
S_5	2	1000	0111	01000
S_6	2	0101	11100	00101
S_7	1	1011	111010	01011
S_8	1	1100	111011	01100
S_9	1	0001	111100	00001
S_{10}	1	1101	111101	01101
S_{11}	1	1111	111110	01111
S_{12}	1	0011	111111	00011
S_{13}	0	1110	-	-
S_{14}	0	1010	-	-
S_{15}	0	1001	-	-



ref: [Jas VTS'99]

LFSR Reseeding

Linear Feedback Shift Register



System of linear equations

$S0 = L1 \oplus L3$
$S1 = L0 \oplus L1 \oplus L2$
$S2 = L1 \oplus L2 \oplus L3$
$S3 = L0 \oplus L1 \oplus L2 \oplus L3$
$S4 = L0 \oplus L2 \oplus L3$
$S5 = L0 \oplus L3$
$S6 = L0$
$S7 = L1$
$S8 = L2$
$S9 = L3$

Test Cube = 1 X X X 0 1 X X 1 0

$S9 = 0 = L3$
$S8 = 1 = L2$
$S5 = 1 = L0 \oplus L3 \Rightarrow L0 = 1$
$S4 = 0 = L0 \oplus L2 \oplus L3$
$S0 = 1 = L1 \oplus L3 \Rightarrow L1 = 1$

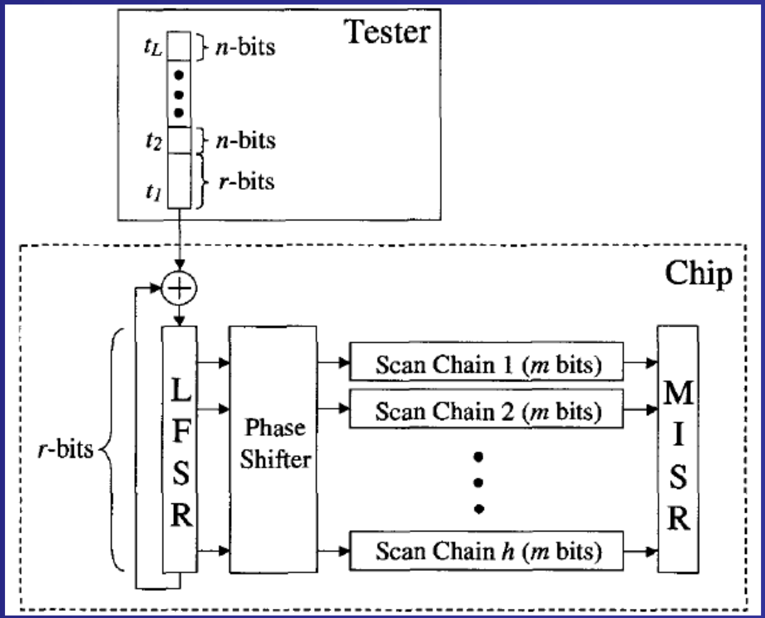
⇓

Seed = 1110

Ref: [Konemann ETC'91]

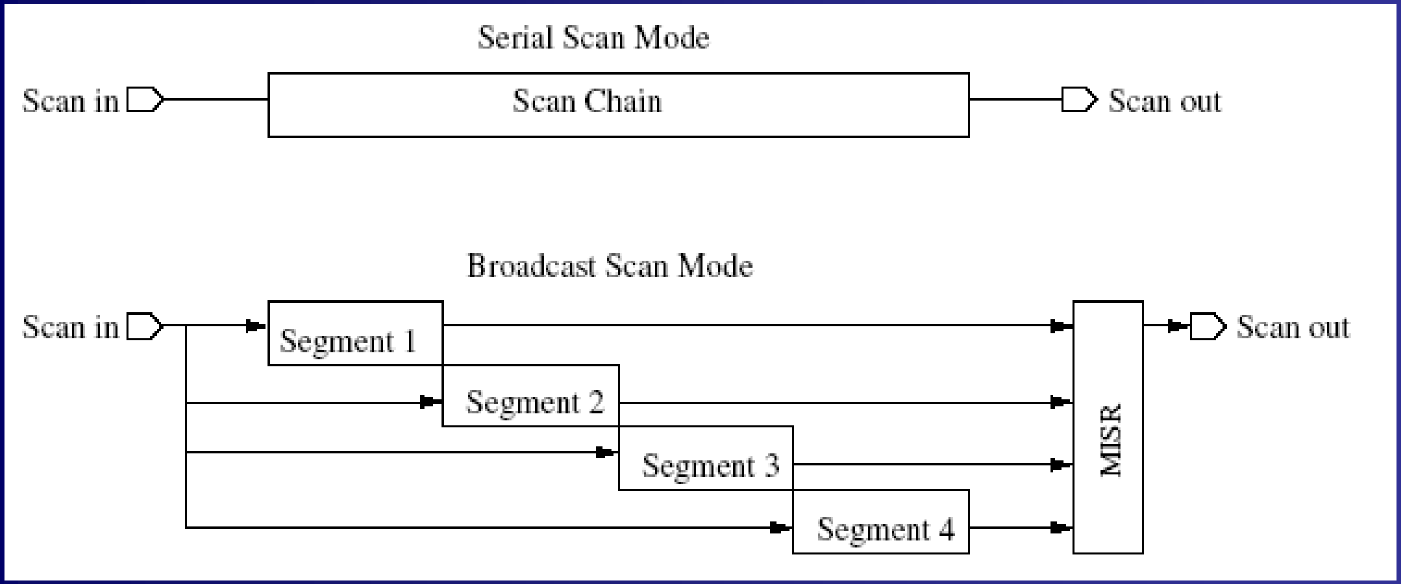
LFSR Reseeding

- Periodically Reseeding - The LFSR size has to be large enough to achieve low probability ($<10^{-6}$) of not finding a seed
  - Single-polynomial LFSR : > Maximum specified bits (Smax) + 20
    - "LFSR-Coded Test Patterns for Scan Design", Konemann ETC'91
  - Multiple-polynomial LFSR : > Smax + 4
    - "Generation of vectors patterns through reseeding of multiple-polynomial LFSR", S. Hellebrand. et.al, ITC'92
- Dynamic reseeding
  - Seed is modified incrementally while test generation proceeds
    - "Test Vector Encoding Using Partial LFSR Reseeding", C.V.Krishna, ITC'01



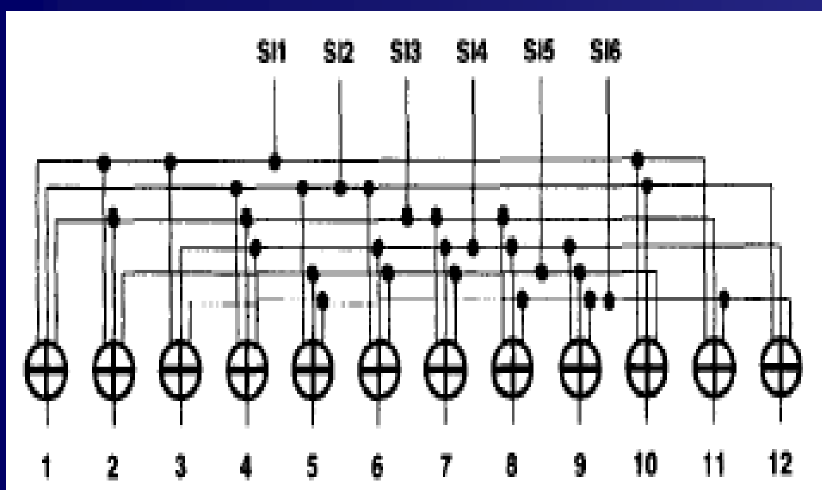
Broadcasting

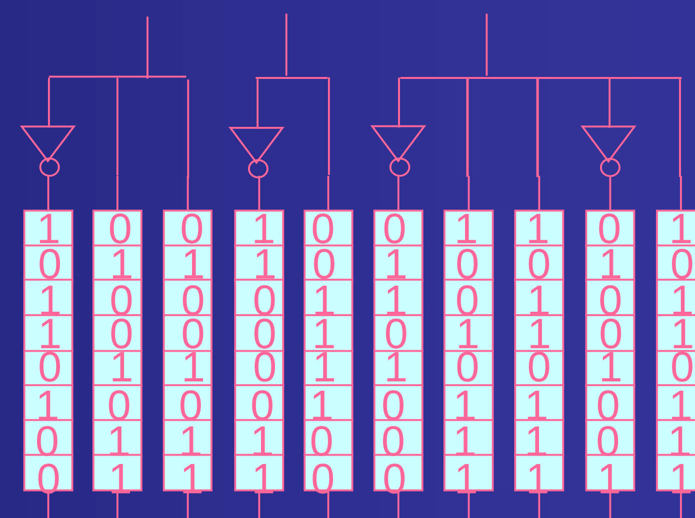
- Illinois Scan
  - One scan line is routed to multiple scan chains
    - "A case study on the implementation of Illinois scan architecture", Hsu, et.al, ITC'01



Continuous-flow Linear Expansion

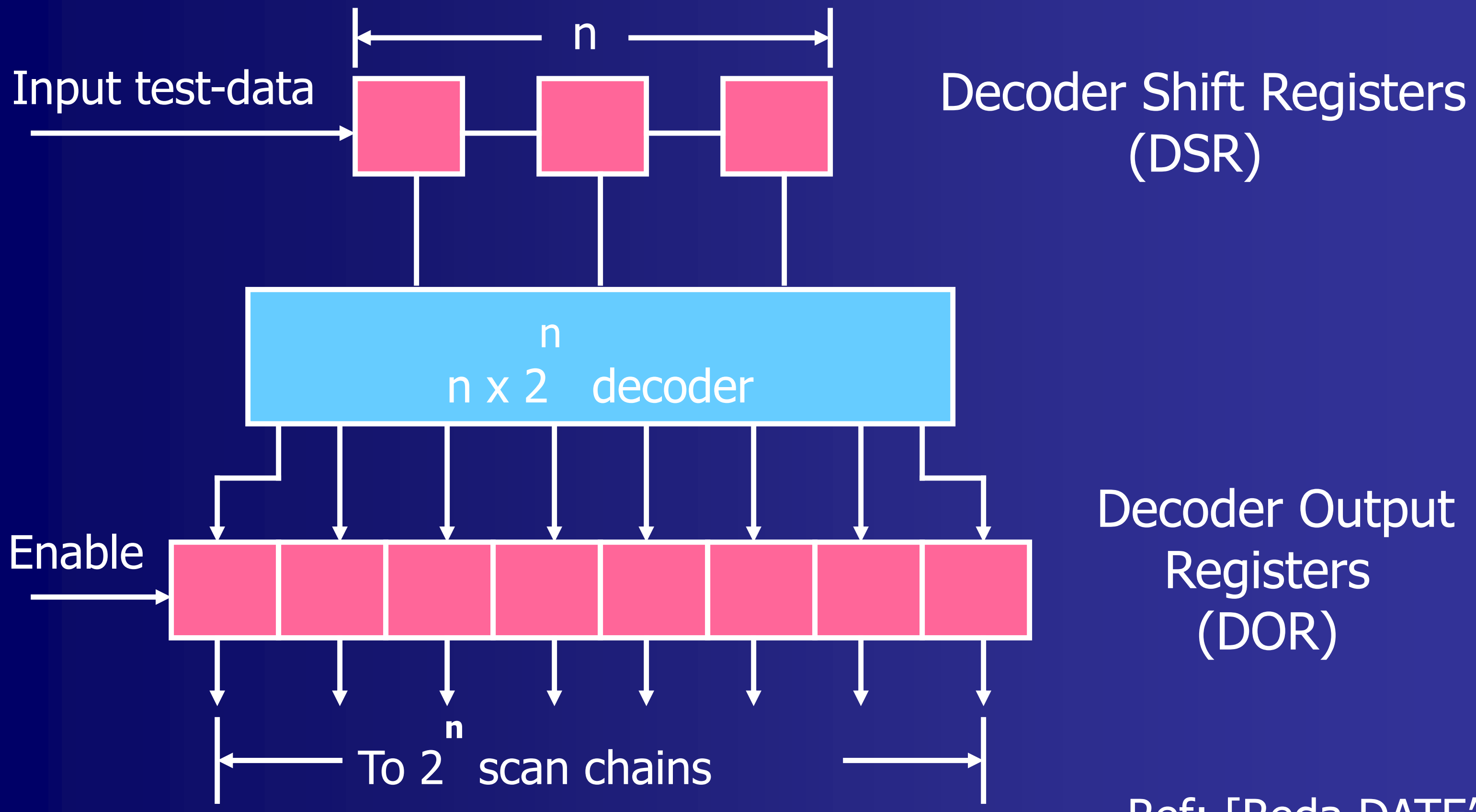
- Use Xor- or inverter- network for de-compression
  - "A SmartBIST Variant with Guaranteed Encoding", Koenemann, ATS'01
  - "Frugal Linear Network-Based Test Decompression for Drastic Test Cost Reductions", Rao ICCAD'03





Mutation

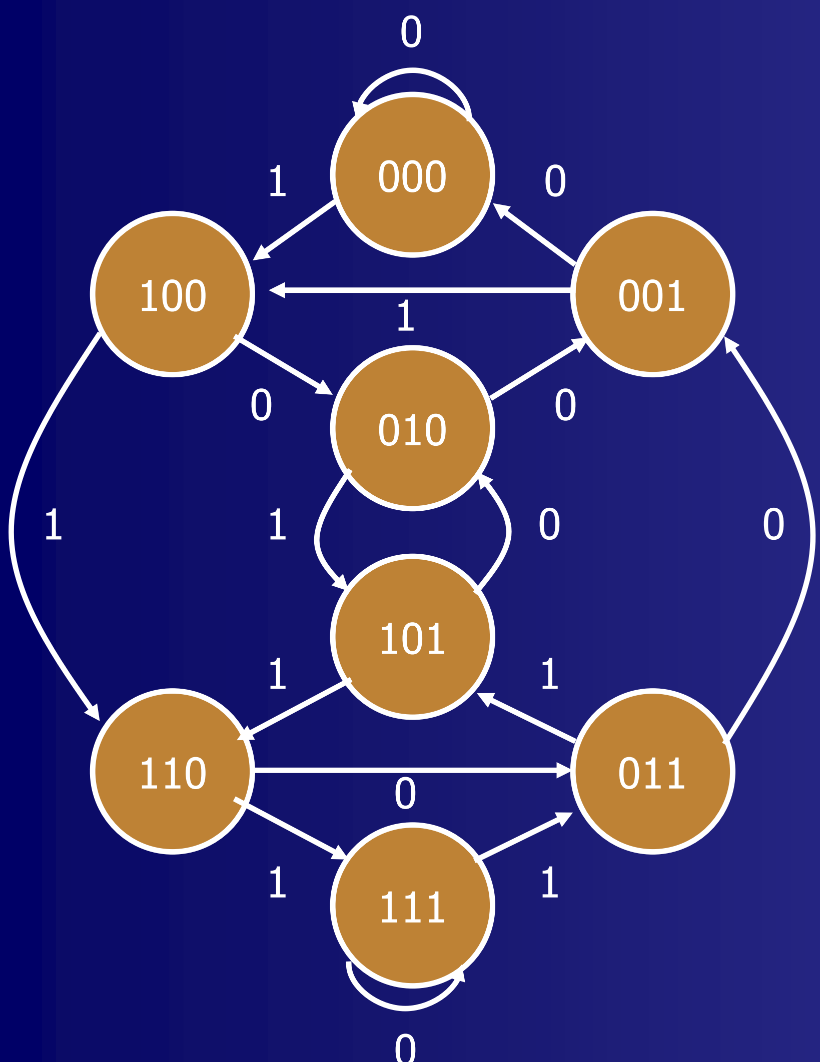
- Supply the current pattern by flipping bits of the last pattern



Ref: [Reda DATE'02]

Mutation

State transition diagram of DSR

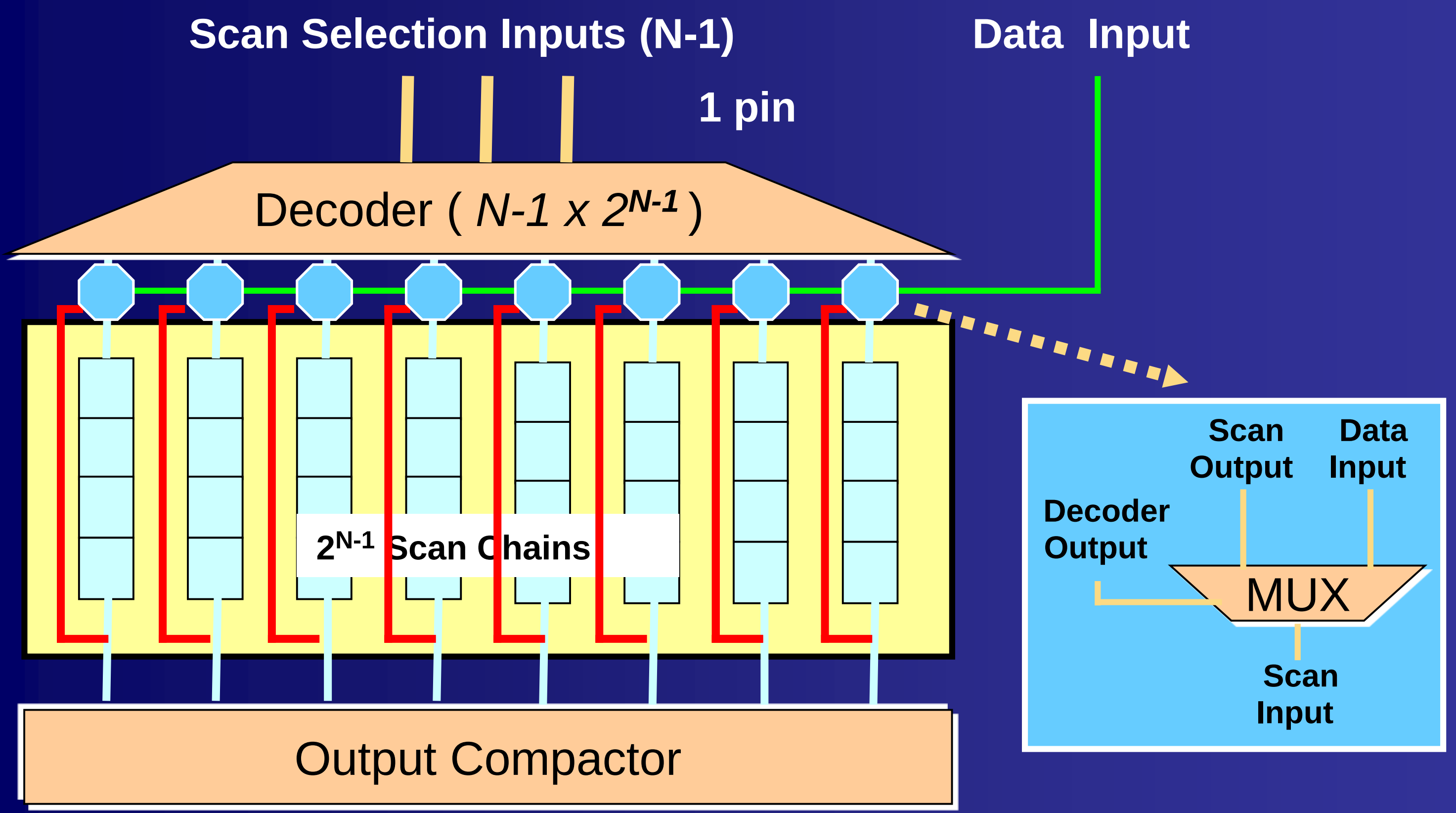


Distance matrix for state transition diagram

	0	1	2	3	4	5	6	7
0	0	3	2	3	1	3	2	3
1	1	0	2	3	1	3	2	3
2	2	1	0	3	2	1	2	3
3	2	1	2	0	2	1	2	3
4	3	2	1	2	0	2	1	2
5	3	2	1	2	3	0	1	2
6	3	2	3	1	3	2	0	1
7	3	2	3	1	3	2	3	0

Mutation

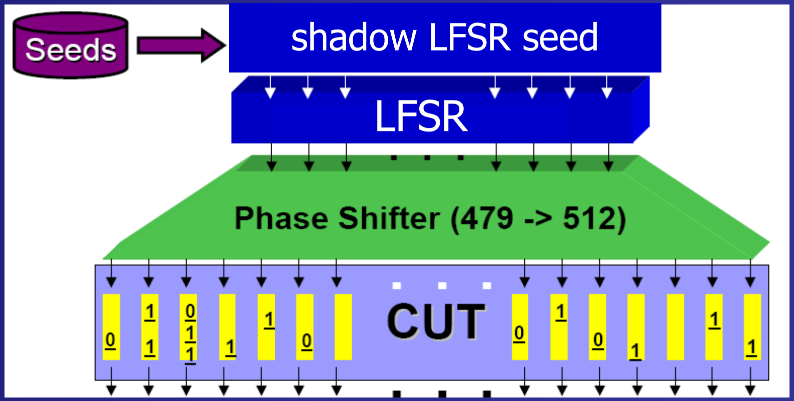
- Circular scan
  - Flip the bits from the captured values



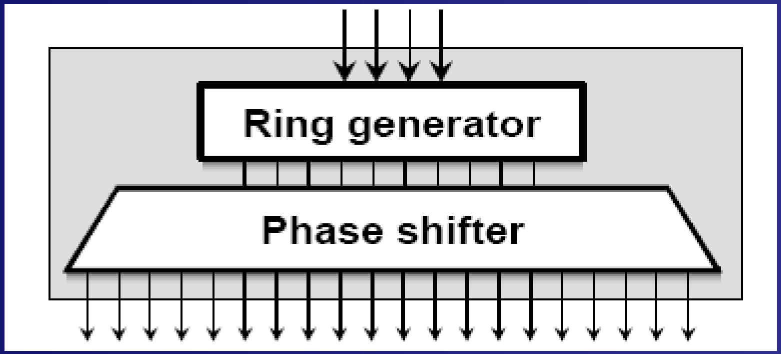
Ref: [Arslan ICCAD’04]

Industrial Tools

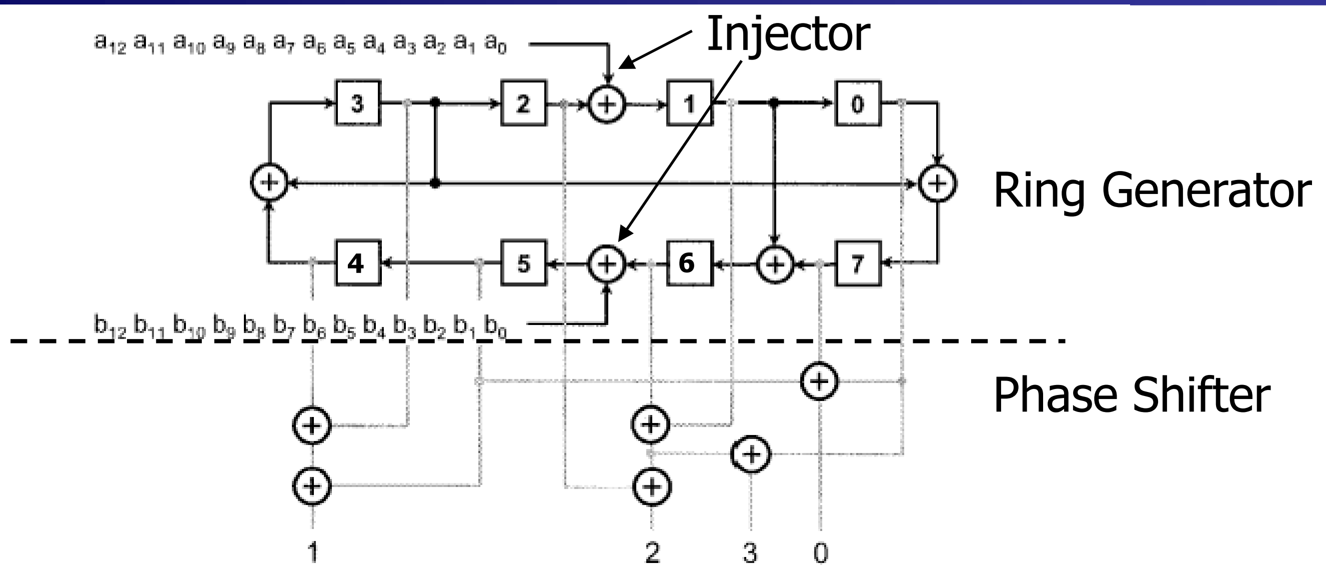
- Synopsys: "XDBIST"
  - LFSR reseeding



- Mentor Graphics: "TestKompress" (EDT)
  - Test cubes are compacted prior to random fill, random fill is achieved through decompression



TestKompress



Example of four-output 8-bit decompressor.

TABLE I
EQUATIONS ASSOCIATED WITH DECOMPRESSOR CELLS FOR FIRST SEVEN CYCLES

	cycle	0	1	2	3	4	5	6	7
V0	0	0	a_0	0	0	0	b_0	0	0
		a_0	a_1	0	0	b_0	b_1	a_0	0
		a_1	a_2	0	b_0	b_1	$a_0 \oplus b_2$	a_1	a_0
	3	a_2	a_3	b_0	$b_1 \oplus b_0$	$a_0 \oplus b_2$	$a_1 \oplus b_3$	$a_2 \oplus a_0$	$a_1 \oplus b_0$
L		a_3	$a_4 \oplus b_0$	$b_1 \oplus b_0$	$a_0 \oplus b_2 \oplus b_1 \oplus b_0$	$a_1 \oplus b_3$	$a_2 \oplus a_0 \oplus b_4$	$a_3 \oplus a_1 \oplus b_0$	$a_2 \oplus b_1 \oplus b_0$
		$a_4 \oplus b_0$	$a_5 \oplus b_1 \oplus b_0$	$a_0 \oplus b_2 \oplus b_1 \oplus b_0$	$a_1 \oplus a_0 \oplus b_3 \oplus b_2 \oplus b_1 \oplus b_0$	$a_2 \oplus a_0 \oplus b_4$	$a_3 \oplus a_1 \oplus b_5 \oplus b_0$	$a_4 \oplus a_2 \oplus b_1$	$a_3 \oplus a_0 \oplus b_2 \oplus b_1 \oplus b_0$
	6	$a_5 \oplus b_1 \oplus b_0$	$a_6 \oplus a_0 \oplus b_2 \oplus b_1 \oplus b_0$	$a_1 \oplus a_0 \oplus b_3 \oplus b_2 \oplus b_1 \oplus b_0$	$a_2 \oplus a_1 \oplus b_4 \oplus b_3 \oplus b_2 \oplus b_1 \oplus b_0$	$a_3 \oplus a_1 \oplus b_5 \oplus b_0$	$a_4 \oplus a_2 \oplus b_6 \oplus b_1$	$a_5 \oplus a_3 \oplus a_0 \oplus b_2$	$a_4 \oplus a_1 \oplus a_0 \oplus b_3 \oplus b_2 \oplus b_1$

TestKompress

- System of linear equations

EQUATIONS ASSOCIATED WITH FIRST THREE CELLS OF EACH SCAN CHAIN

cycle	S.0	S.1	S.2	S.3
4	$a_3 \oplus a_0 \oplus b_4 \oplus b_1 \oplus b_0$	$a_3 \oplus a_2 \oplus a_1 \oplus b_4 \oplus b_2 \oplus b_1$	$a_4 \oplus a_1 \oplus b_3 \oplus b_1$	$a_4 \oplus a_3 \oplus a_1 \oplus b_3 \oplus b_0$
5	$a_4 \oplus a_1 \oplus a_0 \oplus b_5 \oplus b_2 \oplus b_1 \oplus b_0$	$a_4 \oplus a_3 \oplus a_2 \oplus a_0 \oplus b_5 \oplus b_3 \oplus b_2$	$a_5 \oplus a_2 \oplus b_4 \oplus b_2$	$a_5 \oplus a_4 \oplus a_2 \oplus a_0 \oplus b_4 \oplus b_1$
6	$a_5 \oplus a_2 \oplus a_1 \oplus a_0 \oplus b_6 \oplus b_3 \oplus b_2 \oplus b_1$	$a_5 \oplus a_4 \oplus a_3 \oplus a_1 \oplus a_0 \oplus b_6 \oplus b_4 \oplus b_3 \oplus b_0$	$a_6 \oplus a_3 \oplus b_5 \oplus b_3 \oplus b_0$	$a_6 \oplus a_5 \oplus a_3 \oplus a_1 \oplus a_0 \oplus b_5 \oplus b_2 \oplus b_0$

cycle	. . .			8	7	6	5	4
x	x	x	x	x	x	1	x	1
1	x	x	0	x	1	1	x	x
x	x	x	x	x	x	x	x	x
0	0	x	x	1	x	x	0	x

Test cubes

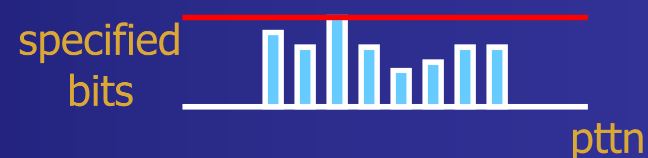
$$a_3 \oplus a_0 \oplus b_4 \oplus b_1 \oplus b_0 = 1$$
$$a_5 \oplus a_4 \oplus a_2 \oplus a_0 \oplus b_4 \oplus b_1 = 0$$
$$a_5 \oplus a_2 \oplus a_1 \oplus a_0 \oplus b_6 \oplus b_3 \oplus b_2 \oplus b_1 \oplus b_0 = 1$$
$$a_5 \oplus a_4 \oplus a_3 \oplus a_1 \oplus a_0 \oplus b_6 \oplus b_4 \oplus b_3 \oplus b_0 = 1$$
$$a_8 \oplus a_7 \oplus a_5 \oplus a_3 \oplus a_2 \oplus b_7 \oplus b_4 \oplus b_2 = 1$$
$$a_6 \oplus a_5 \oplus a_4 \oplus a_2 \oplus a_1 \oplus a_0 \oplus b_7 \oplus b_5 \oplus b_4 \oplus b_4 \oplus b_1 \oplus b_1 \oplus b_0 = 1$$
$$a_8 \oplus a_7 \oplus a_6 \oplus a_4 \oplus a_3 \oplus a_2 \oplus a_1 \oplus a_0 \oplus b_9 \oplus b_7 \oplus b_6 \oplus b_3 \oplus b_2 \oplus b_0 = 0$$
$$a_{11} \oplus a_{10} \oplus a_8 \oplus a_6 \oplus a_5 \oplus a_1 \oplus b_{10} \oplus b_7 \oplus b_5 \oplus b_1 = 0$$
$$a_{11} \oplus a_{10} \oplus a_9 \oplus a_7 \oplus a_6 \oplus a_5 \oplus a_4 \oplus a_3 \oplus a_2 \oplus b_{12} \oplus b_{10} \oplus b_9 \oplus b_6 \oplus b_5 \oplus b_3 = 1$$
$$a_{12} \oplus a_{11} \oplus a_9 \oplus a_7 \oplus a_6 \oplus a_2 \oplus a_0 \oplus b_{11} \oplus b_8 \oplus b_6 \oplus b_2 = 0.$$

cycle	.	.	.	.	.	.	.	4	3	2	1	0	
a :	0	0	0	0	0	0	0	0	0	1	1	0	$\rightarrow$
b :	0	0	0	0	0	1	0	0	1	0	1	0	$\rightarrow$

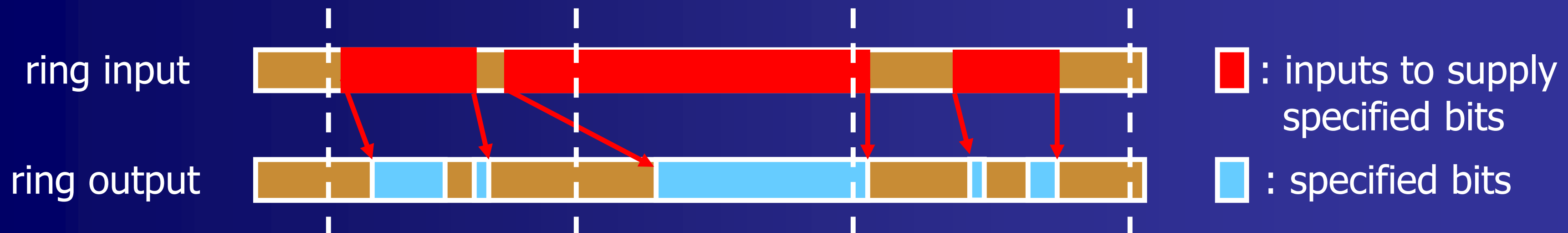
0	1	1	1	1	0	$\underline{1}$	0	$\underline{1}$
$\underline{1}$	0	0	$\underline{0}$	0	$\underline{1}$	$\underline{1}$	0	1
0	0	0	1	1	0	1	1	1
$\underline{0}$	$\underline{0}$	1	1	$\underline{1}$	1	1	$\underline{0}$	0

LFSR Reseeding vs. Ring Generator

- LFSR Reseeding
  - LFSR depth (seed length) is determined by the pattern with most specified bits
  - Attempt to lower the most specified bits of a pattern rather than average specified-bit %



- Ring generator
  - An input bit determines outputs for *d* (depth) cycles
  - Ring depth is determined by the congestion of specified bits over a period of time



Low-power Decompression Scheme

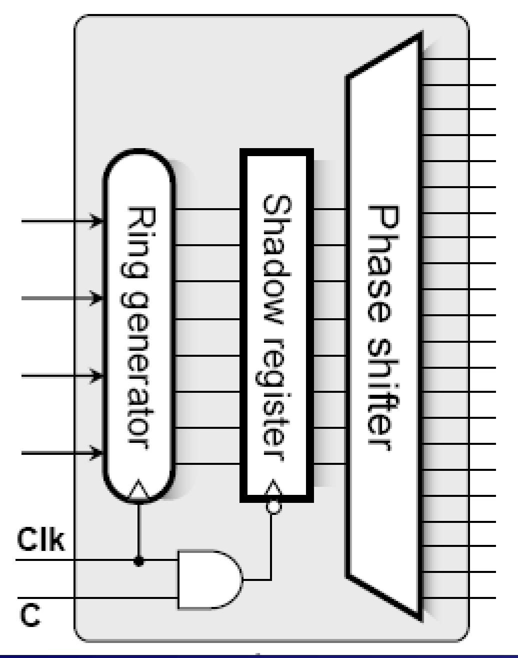
- More scan cells lead to higher power consumption during scan-shifting
- Attempt to minimize scan-value switching during decompression
- Mutation-based decompression is good for low-power scan testing
  - but low compression ratio
- LFSR reseeding or ring generator may achieve high compression ratio
  - but produce a lot switching due to random-fill nature
- Recent low-power decompression schemes
  - Low Power EDT (DAC'07)

Low-Power EDT (1/3)

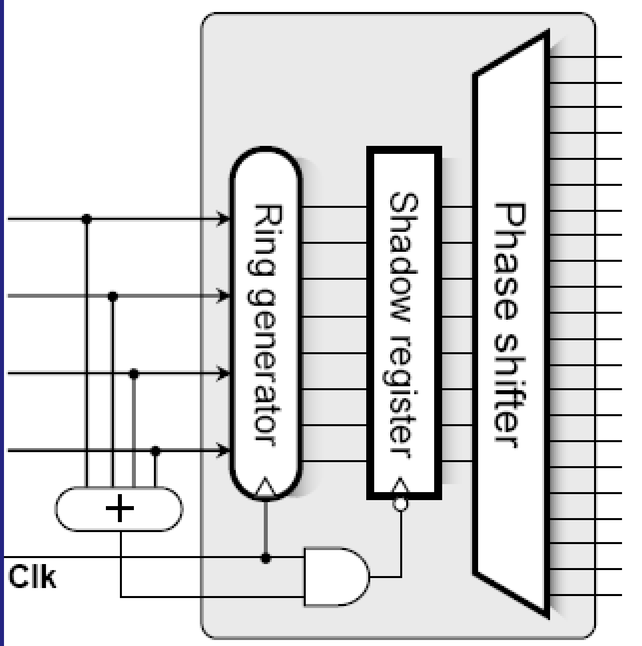
- The basic EDT-based decompressor randomly fill the unspecified bits.
- Main idea is to reduce the fill rate.
  - Let successive unspecified bits have the same value
  - Need a mechanism to sustain the outputs of a decompressor for more than a single clock cycle

Low-Power EDT (2/3)

- A ***shadow register*** *can* save the preceding decompression information and set a desired state of ring generator



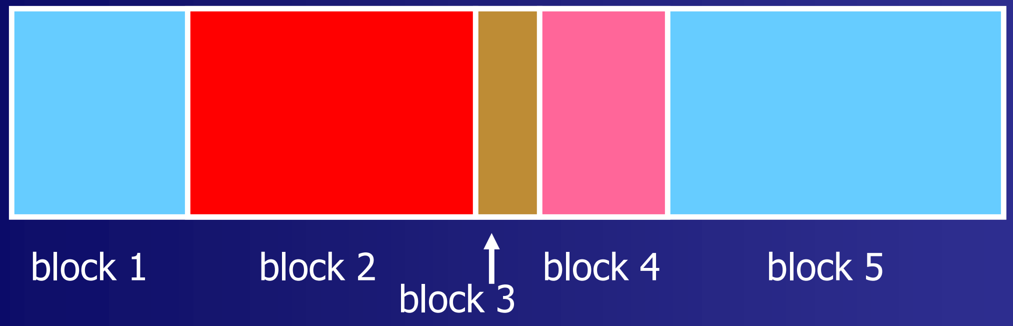
Need additional channel to control shadow register



Merge control bits with original input channels

Low-Power EDT (3/3)

- To further reduce the switching activity, it partitions the original test cube into several blocks comprising consecutive slices
  - Allow one to repeat a given decompressor state many times in succession
- The actual block size is determined by the ability to encode the specified bits occurring within boundaries of the block
- As a result, we can achieve virtually the smallest number of blocks that cover the entire test cube



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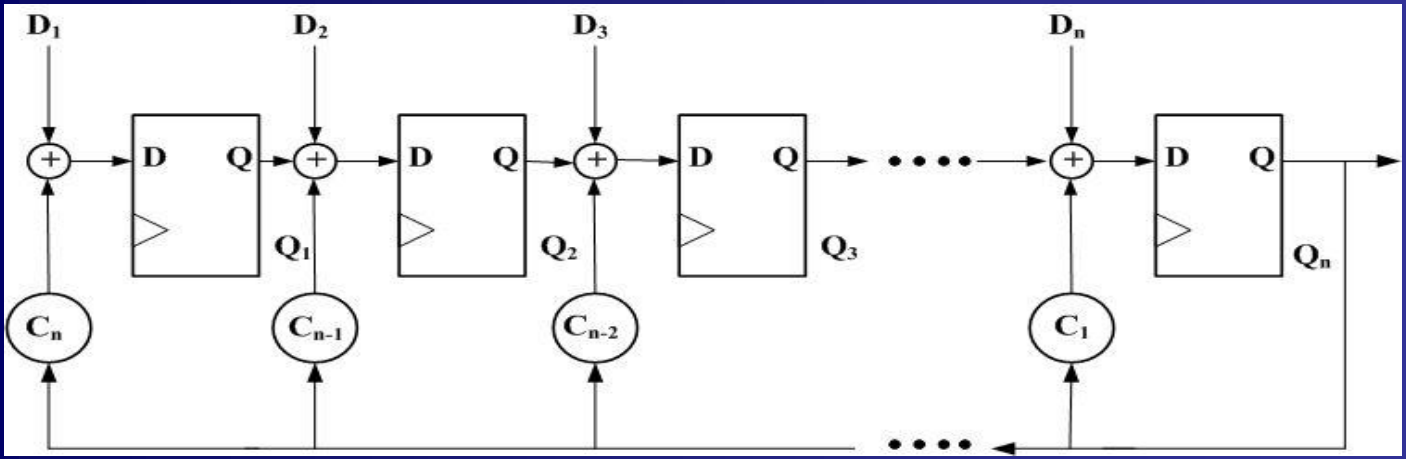
Output-Response Compaction

- Key barrier to effective test response compaction: unknown values among good-circuit results
- If no unknown value,
  – MISR (Multiple Input Signature Registers) can compress an infinitely long output sequence into a fixed-length signature



Unknown Values

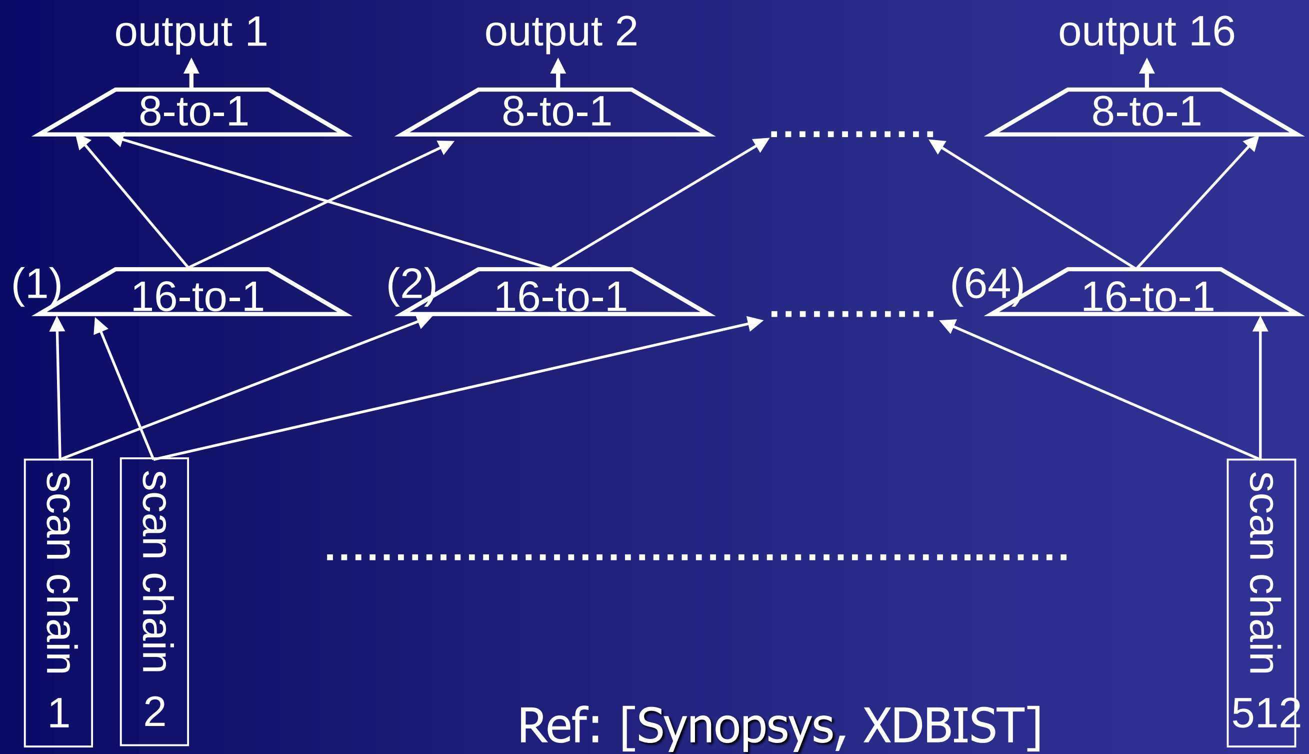
- Definition: the good-circuit response which cannot be calculated by the simulator
- Source of unknown values
  - Un-initialized flip-flops
  - Bus contention
  - Floating bus
  - Multi-cycle paths
  - Limitation of simulator
- Low percentage of unknown (less than 1%) for most industrial designs

Unknown-Tolerant Compaction Scheme

- Selective compactor
- Unknown-blocking MISRs
- Space compactor
- Hybrid compaction scheme

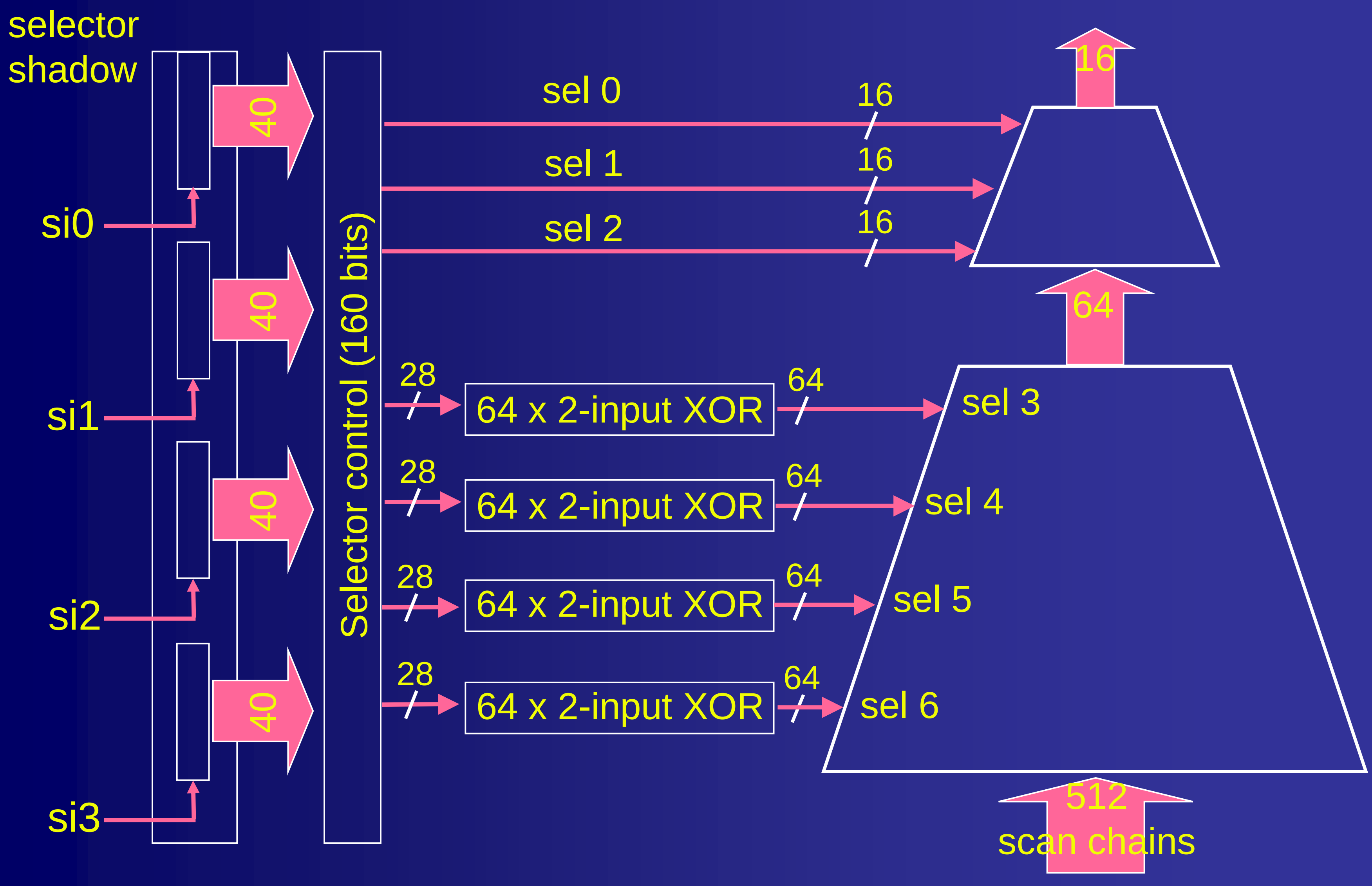
Unknown-Tolerant Compaction (1/3) – Selective Compactor

- Observe only the responses with faulty value
- Discard majority of the responses
- Required a customized ATPG
- [Wohl, ITC'03], [Mentor Graphics, EDT]



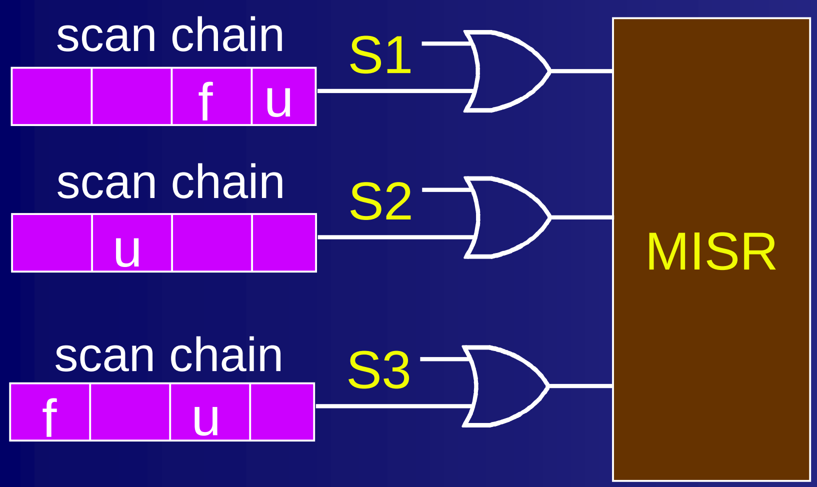
Ref: [Synopsys, XDBIST]

Control Signals for XDBIST



Unknown-Tolerant Compaction (2/3) – Unknown-Blocking MISR

- Block unknowns before feeding into a time compactor
- [Pomeranz, TCAD'04], [Tang, ITC'04], [Chickermane, ITC'04]
- Required pattern-dependent blocking logic or customized ATPG
- Over-mask some known responses



0 : must-observe
1 : blocking (for unknown)

cycle	4	3	2	1
S1	x	x	0	1
S2	x	1	x	x
S3	0	x	1	x

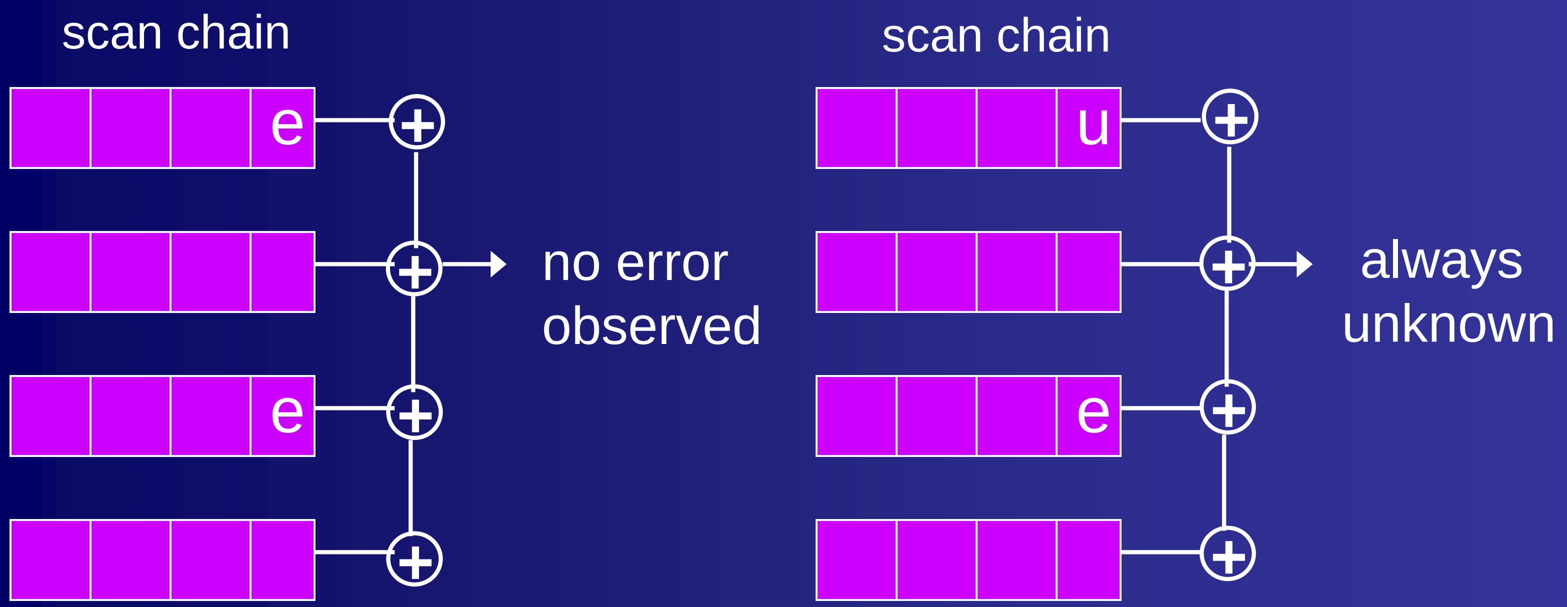
around 50% of the scan-out responses will be blocked !!

Unknown-Tolerant Compaction (3/3)

- Space Compactor
  - Allow unknown values propagating to the compactor
  - Use Xor matrix to reduce the probability that a response is masked by unknowns
  - Pattern-independent HW, APTG-independent flow
- Single-weight Xor matrix
  - X-compact [Mitra, TCAD'02]
- Multiple-weight Xor matrix
  - [Clouqueur ITC'05]
- Xor network with storage elements
  - Block compactor [Wang, ICCAD'03]
  - Convolution compactor, Rajski ITC'03

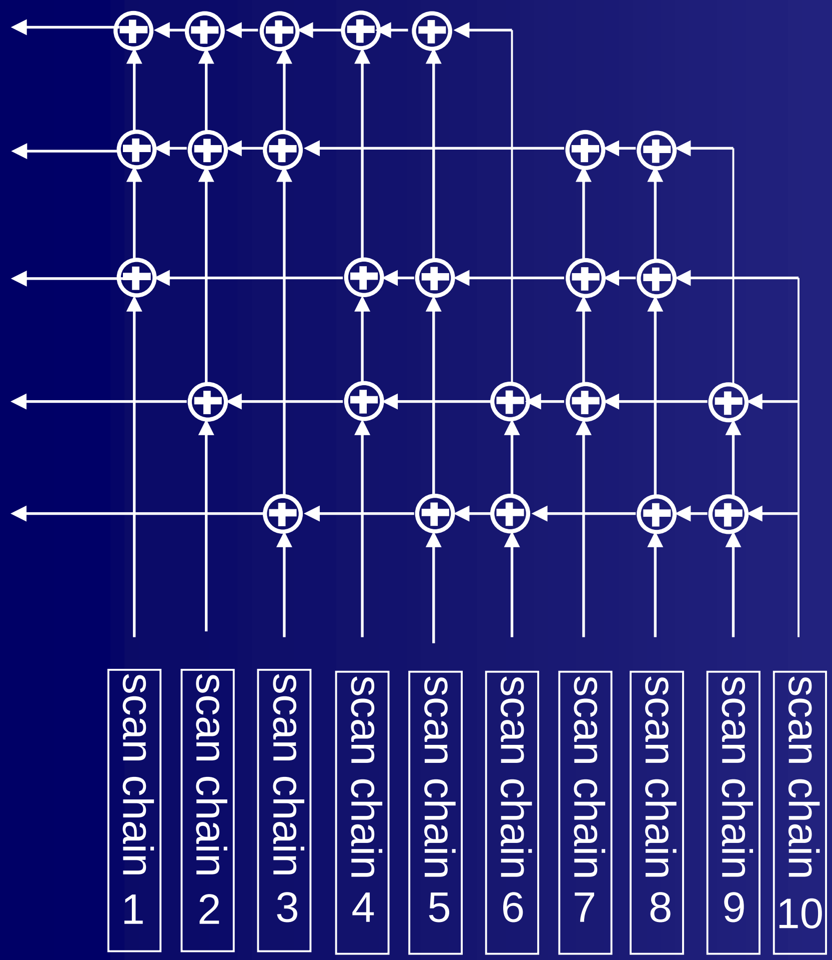
Masking Effects Using XOR Matrix

- Error masking (aliasing)
  - Error (e): different response from good-circuit response
- Unknown-induced masking
  - Unknown (u): unknown response in simulation



X-Compact

5 output

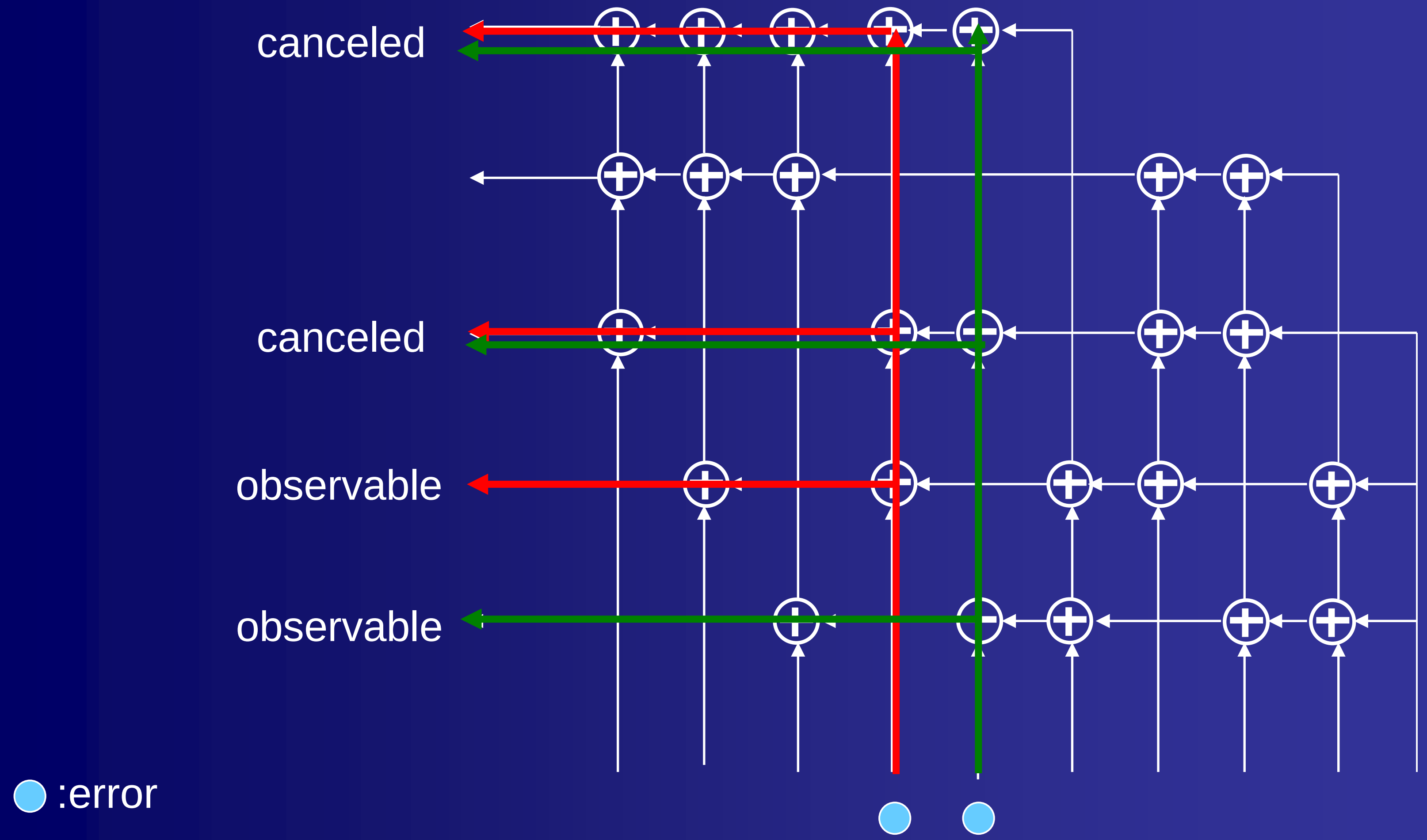


XOR Matrix

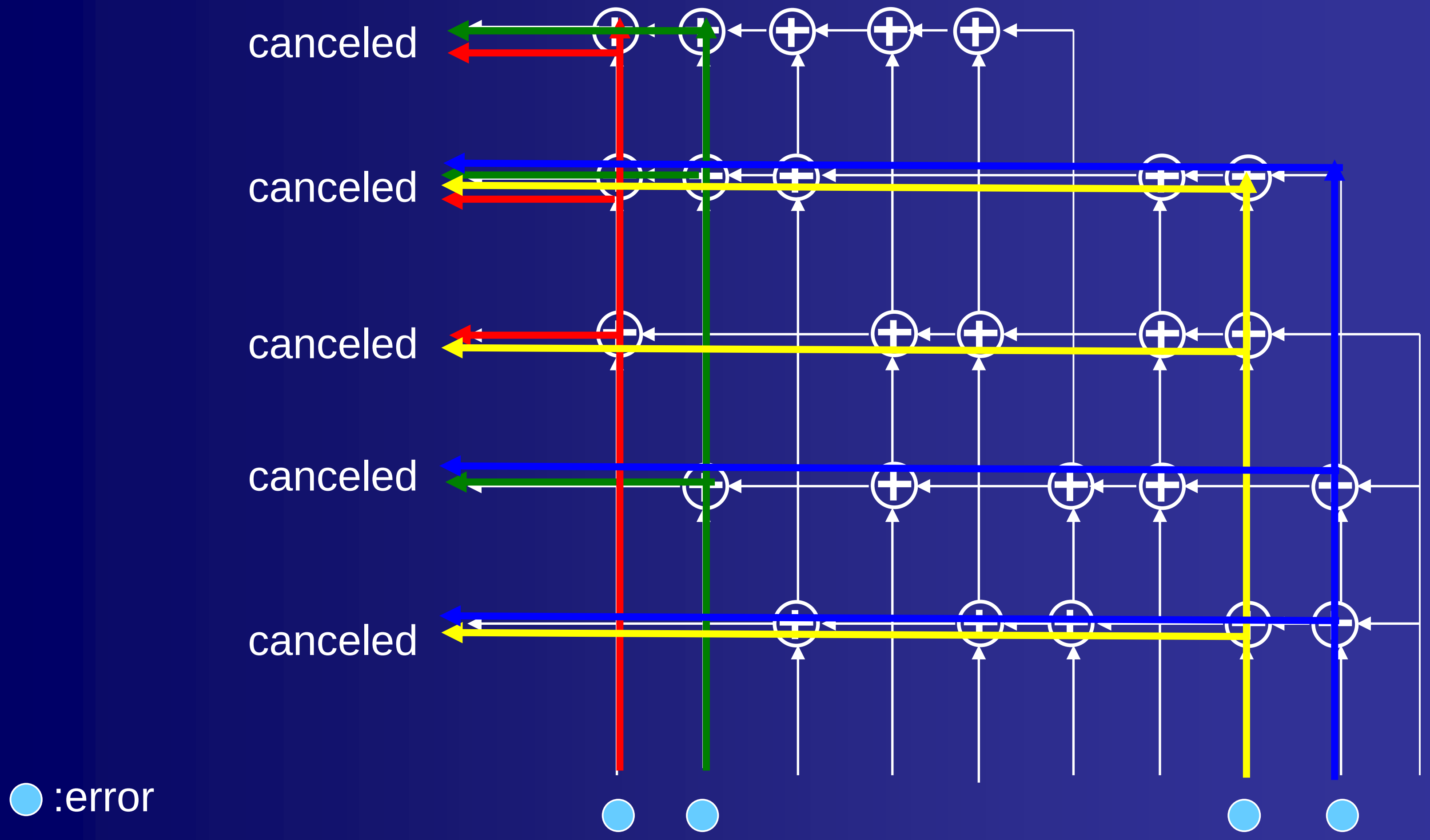
$$\begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \end{pmatrix}$$

- No identical column
- Odd # of 1s for each column
- Can observe 1, 2, or any odd # of errors in the same cycle
- Can observe any 1 error in presence of any 1 unknown

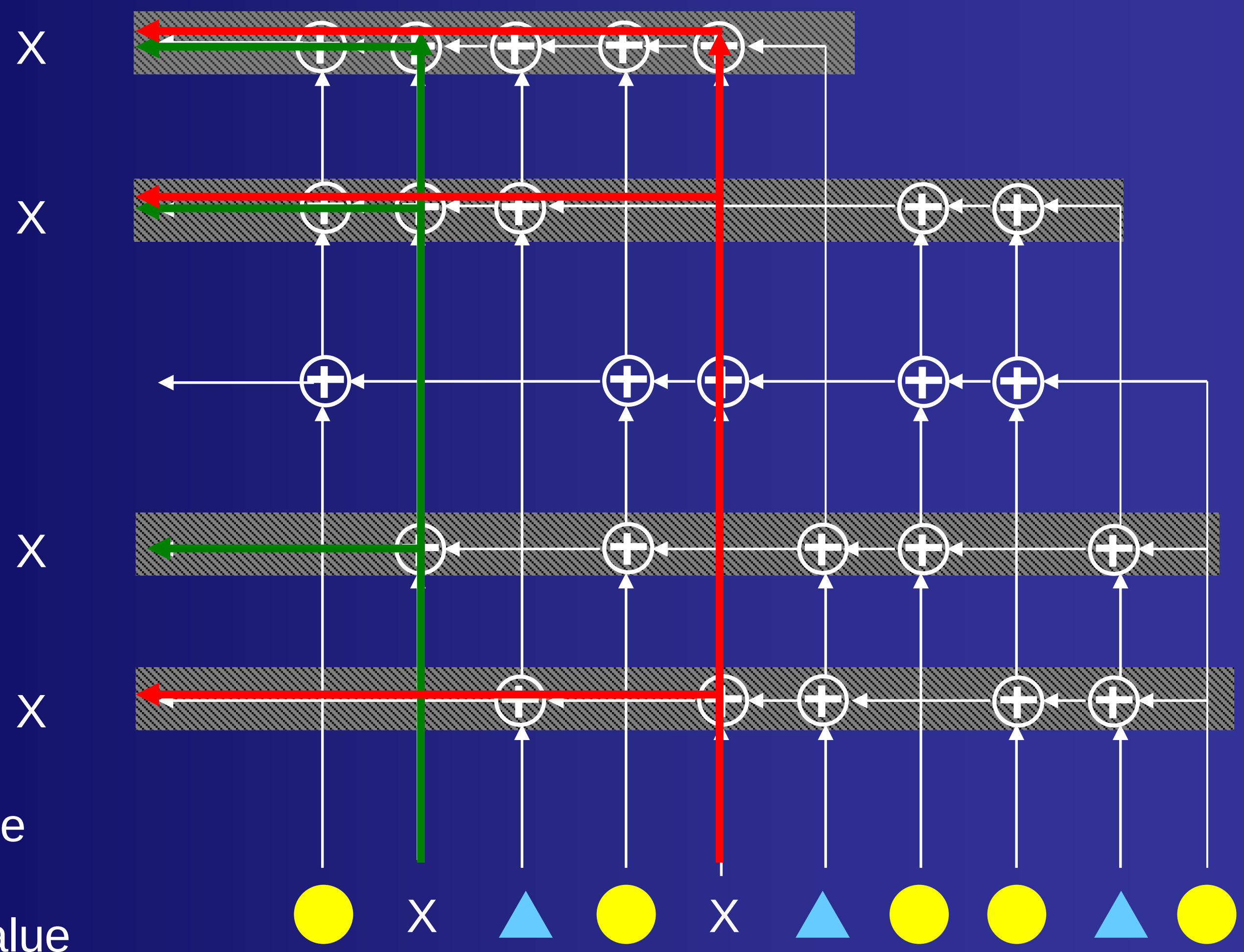
X-Compact



X-Compact



X-Compact

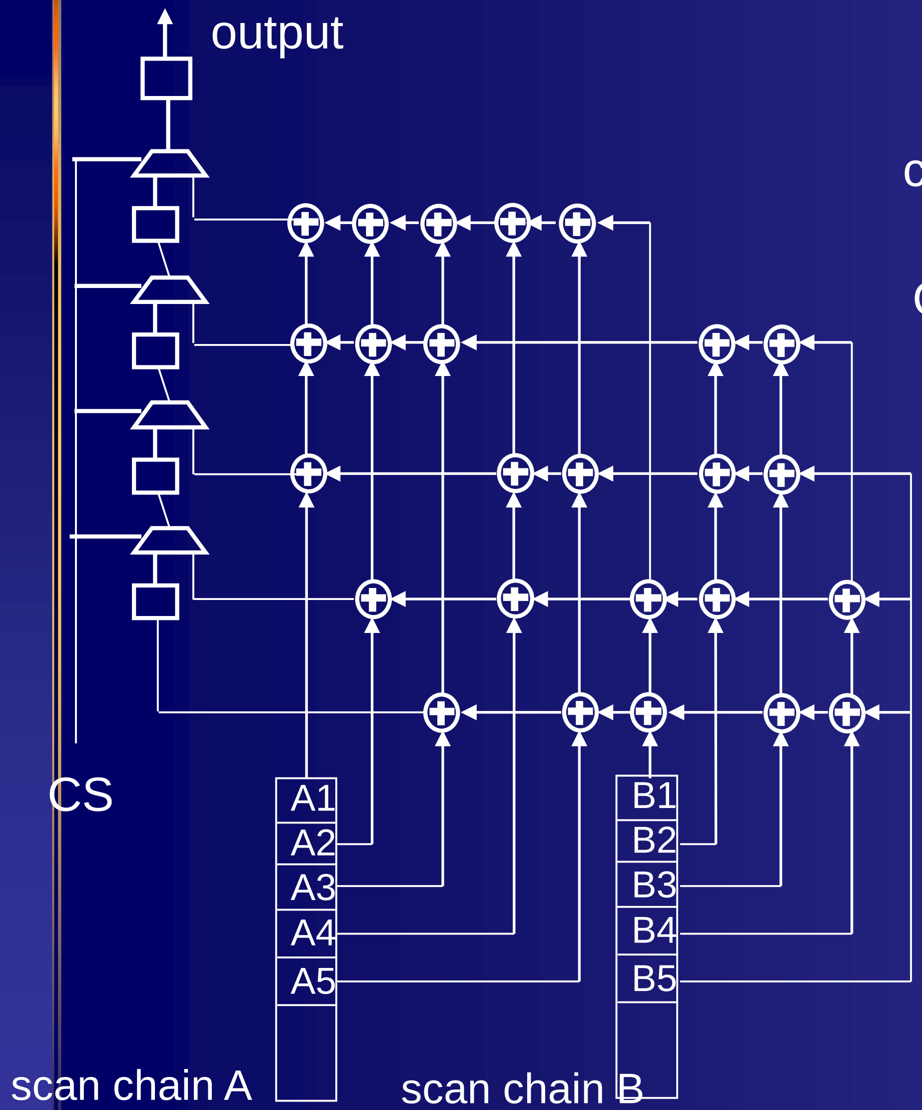


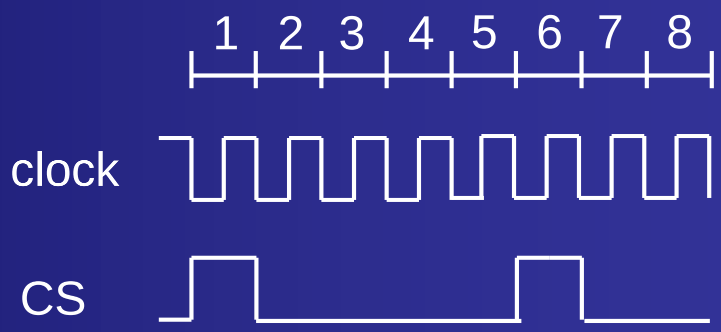
X :unknown value

:observable value

:unobservable value

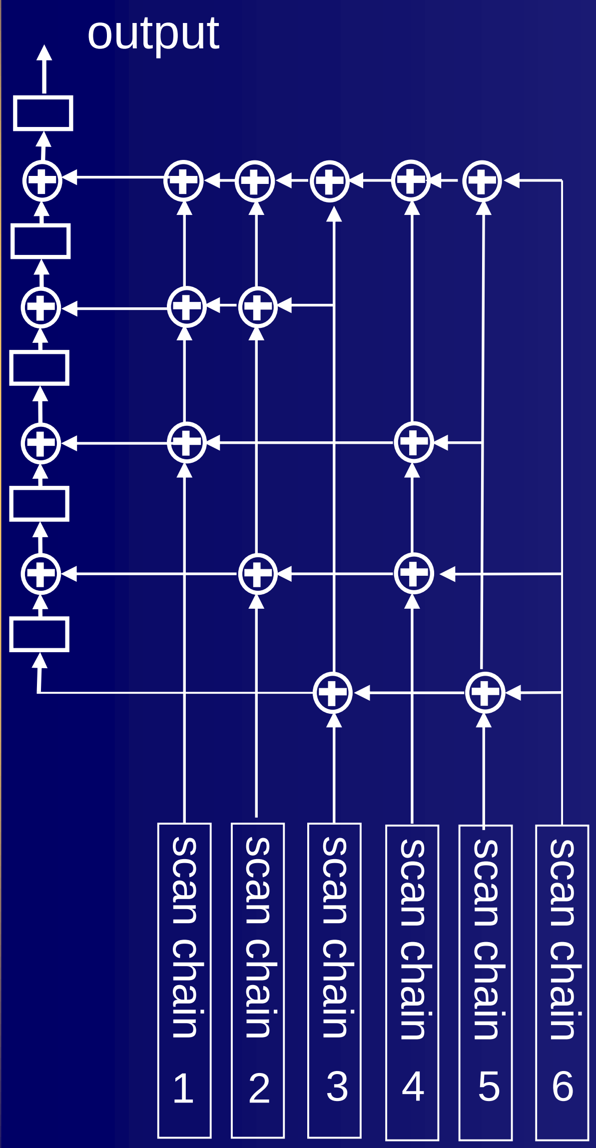
Block Compactor





- When CS=1, FF captures response from XOR matrix
- When CS=0, FF captures response from the FF below it
- The same guarantee for error masking & unknown masking as X-Compact
- Any compaction ratio for any # of scan chains & any # of outputs

Convolution Compactor



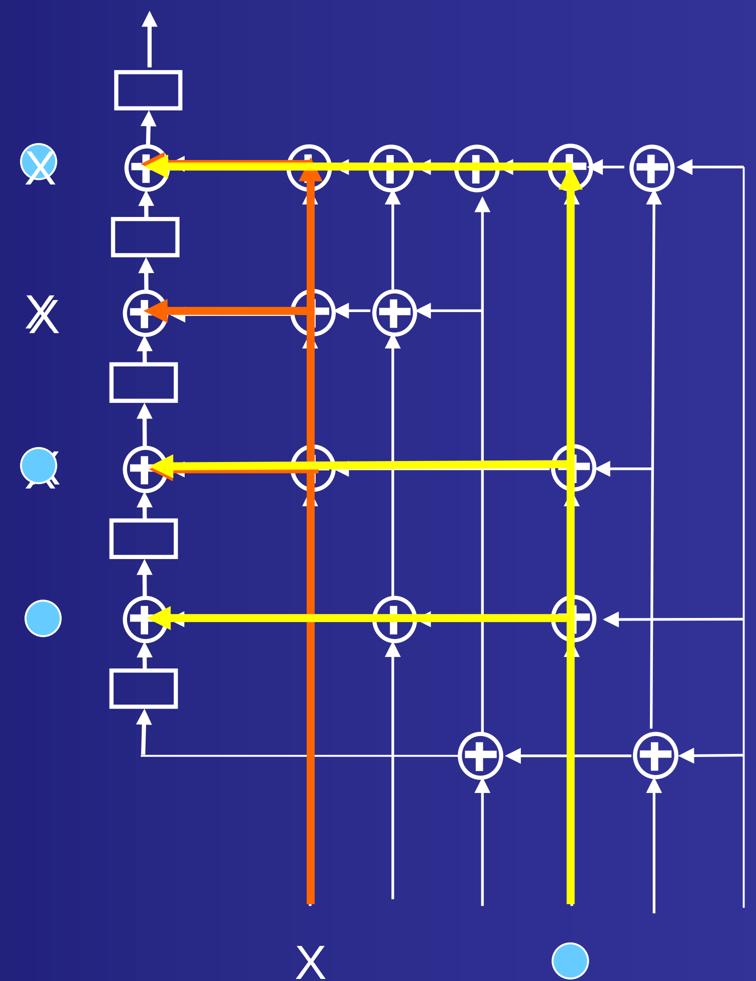
XOR Matrix

$$\begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{pmatrix} \begin{pmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \\ 0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 1 \end{pmatrix}$$

- Same guarantee of error masking and unknown masking with X-Compact
- Any compaction ratio for any # of scan chains & any # of outputs
- Best compaction ratio/hardware overhead

Convolution Compactor

Cycle N+3: Shift



X : unknown value

: error

Diagnosis with Compaction Schemes?

- Selective compactor:
  - Report exact "position" of erroneous responses, i.e., which scan cell captures erroneous response on which pattern
  - Some erroneous responses may miss
- Unknown-blocking MISR:
  - All erroneous responses mix together, worst resolution
  - Report only pass or fail
- Space compactor:
  - Unique faulty syndrome for single error (when no unknown)
  - Lower resolution when multiple errors occur
  - Good for fault-dictionary-based diagnosis
- Suggestion:
  - Should design a by-pass mode in the compaction scheme so that the complete erroneous information can be collected when needed

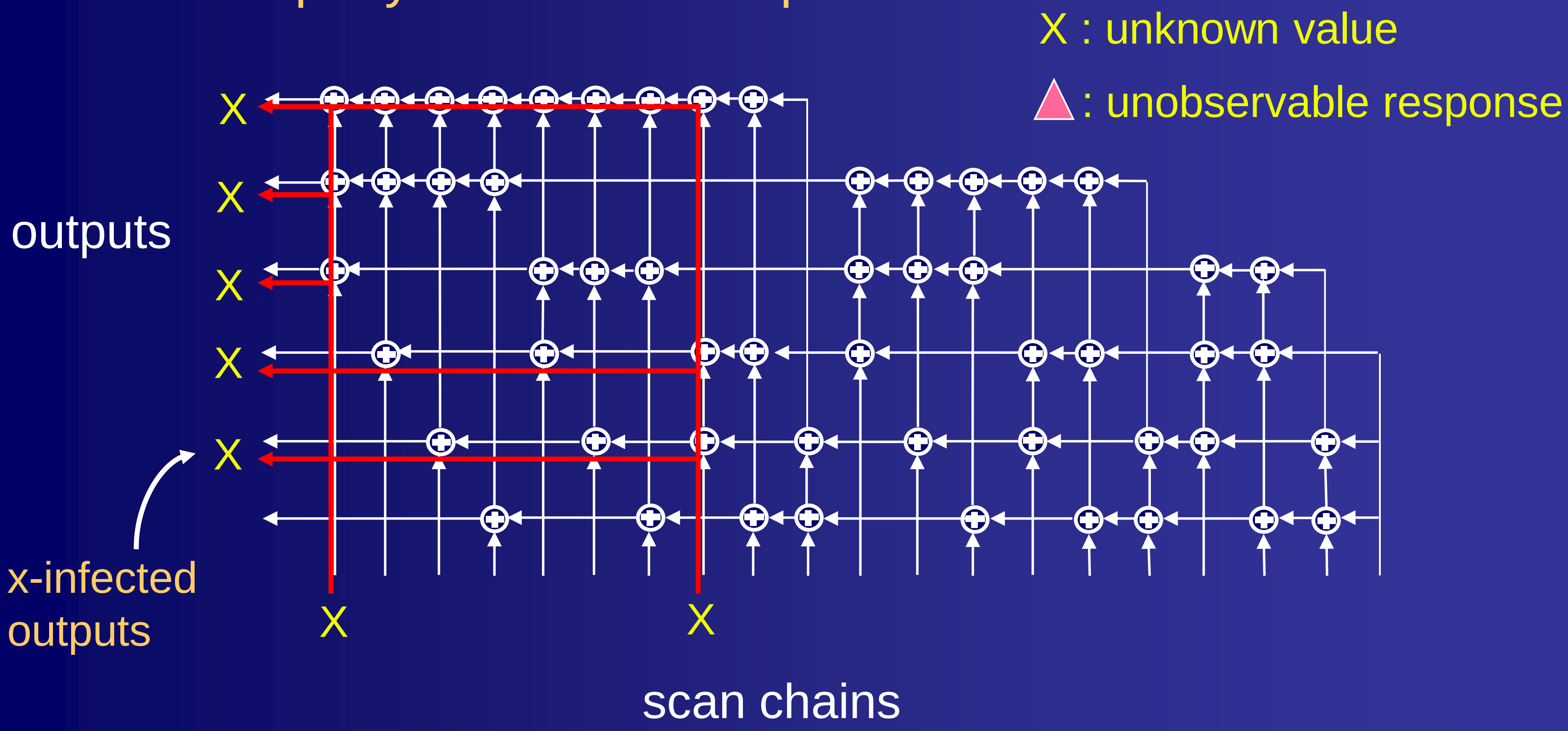
Outline

- Introduction to Scan-based Testing
- Input-Pattern Compression
  - Type of compressions
  - Compression schemes
- Output-Response Compaction
  - Time compactor (MISR)
  - Unknown-tolerant compaction schemes
  - Diagnosis with compactor
- Design optimal space compactor
- Hybrid compaction scheme
- Conclusion

X-induced Masking

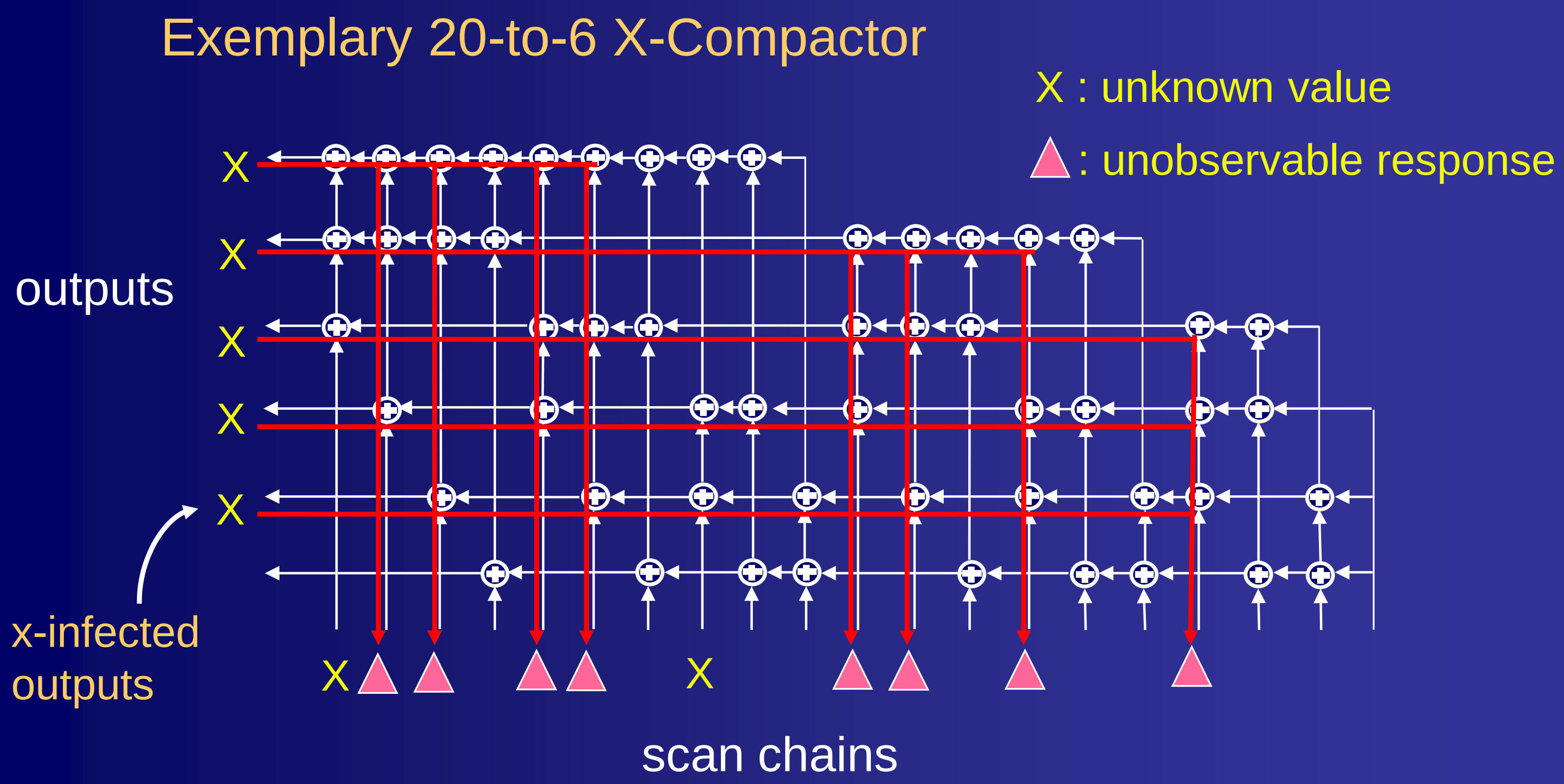
- When multiple unknown values appear
  - Some known responses become unobservable

Exemplary 20-to-6 X-Compactor



X-induced Masking

- When multiple unknown values appear
  - Some known responses become unobservable



Objectives

- Estimate *observable percentage*: percentage of responses being observable in presence of unknowns
- Design a space compactor with maximal compaction ratio and desired observable percentage
- Relate observable percentage to test-quality metric
  - Stuck-at-fault coverage, Bridge Coverage Estimate (BCE)

X-induced Masking vs. Error Masking

- Error masking: multiple errors cancel one another out by Xor operations
- Simple experiment: 50-to-1 simple Xor tree

Circuit	det flt w/o compactor	aliaing flt for a pttn	aliasing flt %	un-det flt with compactor
s35932	43105	35	0.081	0
s38417	39177	18	0.046	0
s38584	42013	16	0.038	0
b17	66638	126	0.189	15

Error masking barely affects fault detection,
but unknown-induced masking does!

Construction Rule for Xor Matrix

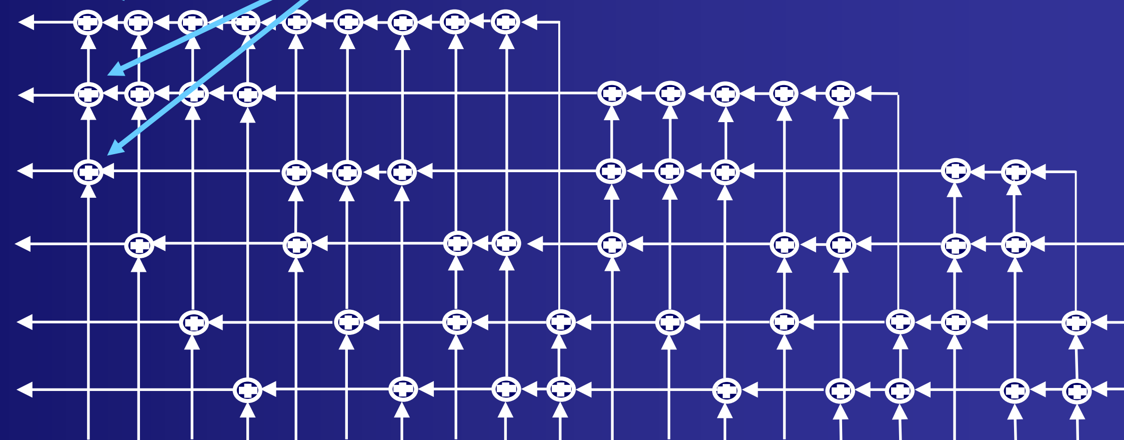
- X-Compact requires:
  - Unique columns in Xor matrix
  - Odd number of Xor gates for each column (*weight*)
  - These two rule only help reducing error masking
- We focus on reducing X-induced masking:
  - Allow identical columns
  - Allow even number of weight

Input/Output Parameters for Equation of Observable Percentage

- Inputs parameters:

W : # of Xor gate per column

M : # of outputs

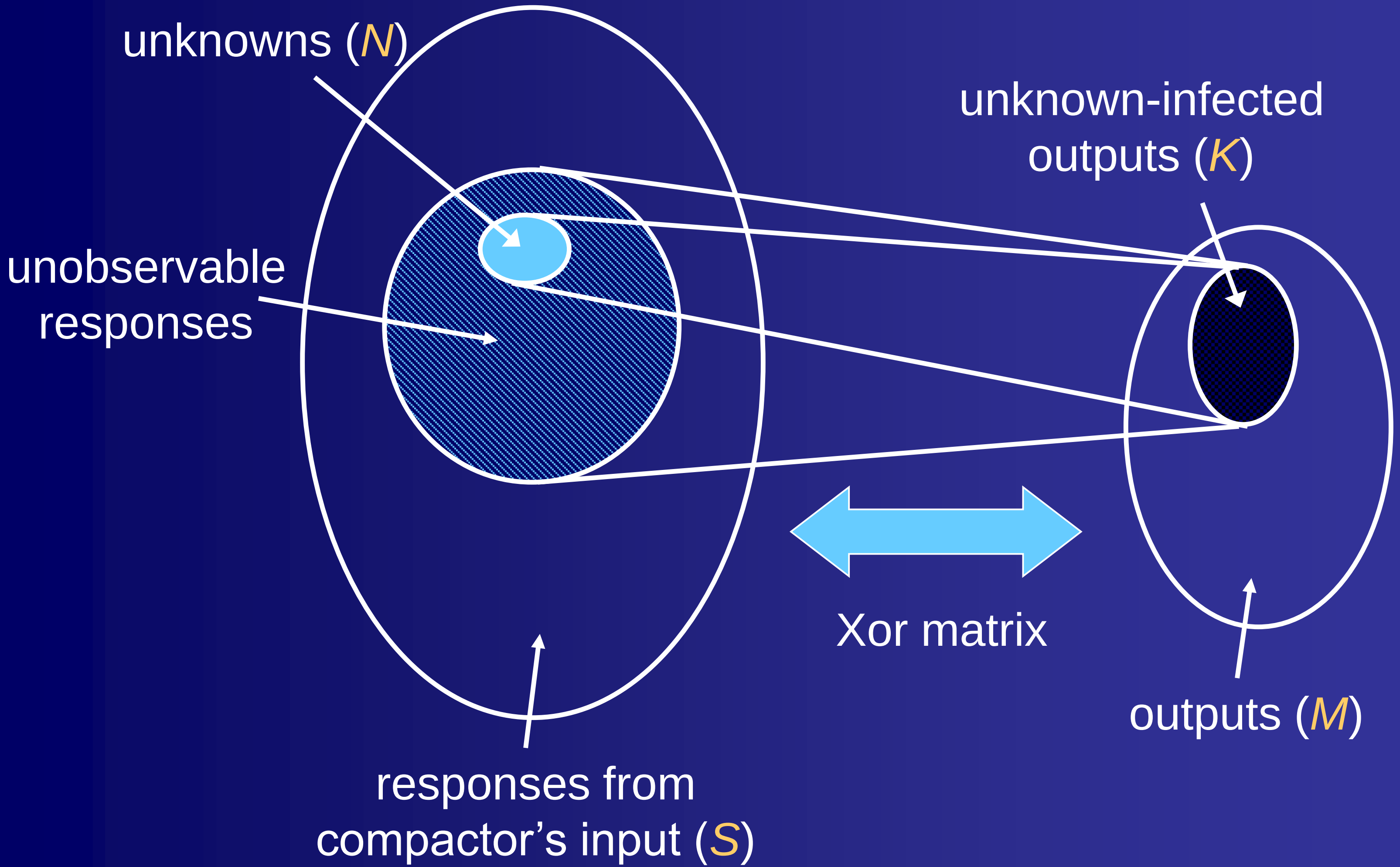


p : unknown % among responses

S : # of responses from scan chains

- Output:
  - *UP* (unobservable percentage)
    - % of responses masked by unknown values
  - *OP* (observable percentage): 1-*UP*

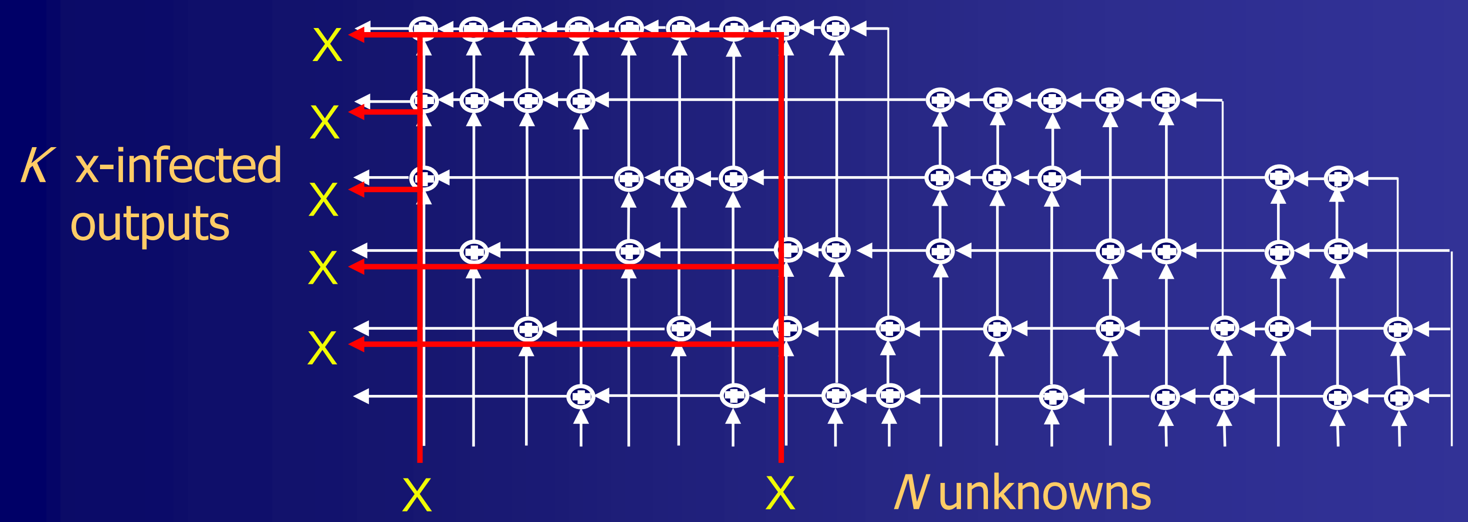
General Concept of our Mathematical Derivation



Mathematical Derivation – Step 1

- Given # of unknowns (*N*), the probability that *K* outputs are x-infected is:

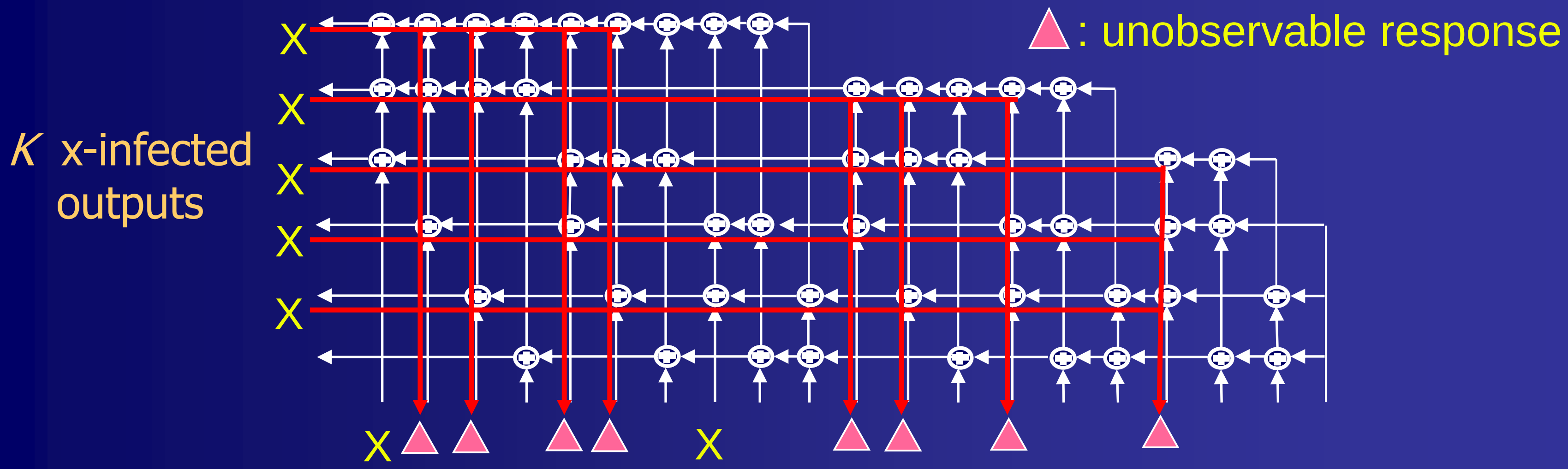
$$\Pr ob\{K = k\} = \frac{\binom{M}{k}}{\binom{M}{W}^N} \sum_{j=W}^{k} (-1)^{k-j} \cdot \binom{k}{j} \cdot \binom{j}{W}^N$$



Mathematical Derivation – Step 2

- Given *K* x-infected outputs, the probability that a response is unobservable is : $f(K) = \dfrac{\binom{K}{W}}{\binom{M}{W}}$
- Its expectation:

$$E[f(K)] = \sum_{k=0}^{M} \frac{\binom{k}{W}}{\binom{M}{W}} \cdot \Pr ob\{K = k\} = \sum_{j=0}^{W} (-1)^j \cdot \frac{\binom{M-j}{W}^N}{\binom{M}{W}^N} \cdot \binom{W}{j}$$



Mathematical Derivation – Step 3

- \# of unknowns at inputs (*N*) is a random variable

$$\Pr ob\{N = n\} = \binom{S}{n} \cdot p^n \cdot (1-p)^{S-n}$$

- So, we re-express the E[*f(K)*] as a function of *N*, then the unobservable percentage (*UP*) is:

$$UP = \sum_{n=0}^{S} \Pr ob\{N = n\} \cdot E_n[f(K)]$$

$$= \sum_{j=0}^{W} (-1)^j \cdot \binom{W}{j} \cdot (p \cdot \frac{\binom{M-j}{W}}{\binom{M}{W}} + 1 - p)^S$$

$$OP = 1 - UP$$

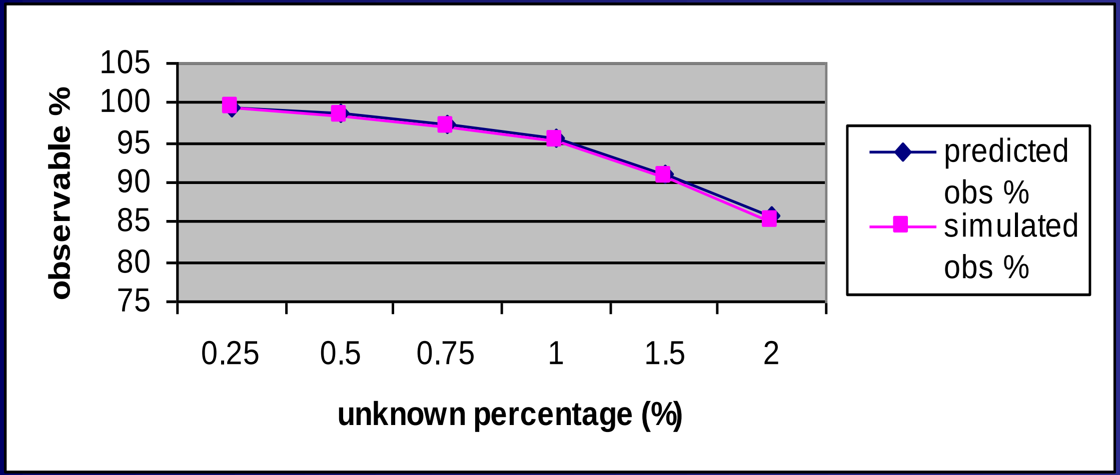
Accuracy Comparison

- Compare prediction results with simulation results
  - 1-million sampling of biased unknowns (90% unknowns come from 10% chains)

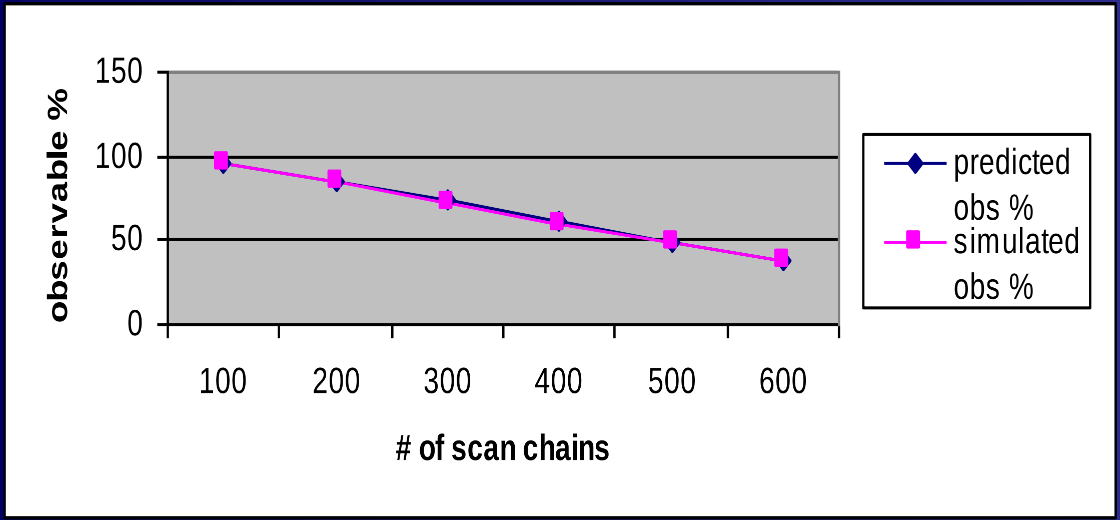
Changing weight
10 outputs, 100 scan chains, 1% unknown

Accuracy Comparison

- Change other parameters



Changing unknown %
10 output
100 scan chains
weight of 3



Changing # of chain
10 output
weight of 3
1% unknown

Designing An Optimal Compactor

Given:

- desired observable %, unknown %, # of outputs

Find:

- *S* : maximal # of supported scan chains
- *W* : optimal weight

# of chain	observable %		
	w=1	w=2	w=3
160	90.49	94.79	94.72
180	89.36	93.87	93.62
200	88.25	92.91	92.45
220	87.15	91.92	91.21
240	86.03	90.89	89.92
260	85.00	89.83	88.57
280	83.94	88.74	87.17

4 output
1% unknown
90% desired obs.%

max_chain = 240,
W = 2

How Much Observable Percentage Is Enough?

- Test-quality metrics used in this work
  - stuck-at-fault coverage, BCE [Benware ITC’03]
- Test quality w.r.t an observable % highly depends on test set and circuit under test

obs. %	10%	30%	50%	70%	90%	95%	100%
b17	74.74	84.93	88.57	90.50	91.62	91.84	92.04
s35932	51.61	78.20	86.24	89.43	91.08	91.34	91.54
s38417	87.10	95.78	97.73	98.80	99.29	99.46	99.53
s38584	77.91	89.29	93.22	95.07	96.06	96.29	96.44

Stuck-at fault coverage w.r.t. observable percentages

Test-Quality Prediction (Stuck-at-fault Coverage & BCE)

- Inputs
  - CUT, test set, a list of observable percentages (*op* s)
- Outputs
  - Stuck-at-fault coverage & BCE for each *op*
- Approach:
  - For each fault f, we collect the following statistics
    - DN_f : total # of patterns detecting fault *f* (*detecting patterns*)
    - ON_f : total # of outputs propagating a faulty value of *f* for entire test set (*faulty outputs*)
  - One-time fault-simulation-based method for all *op* s

Prediction of Stuck-at-fault Coverage

- The probability that a fault can be detected under a given *op* :

$$det\_prob_f = 1 - (1 - op)^{ON_f}$$

- Then, the predicted fault coverage (FC) is:

$$FC = \frac{1}{|F|} \sum_{f \in F} det\_prob_f$$

Prediction of BCE

- Definition: $BCE = \frac{1}{F} \sum_{f \in F} (1 - 0.5^{N_f})$
  - N_f is the # of patterns detecting f ($N_f = DN_f$, when $op = 1.0$)
- For each fault f, we approximate # of outputs containing faulty value for each detecting pattern by its average: ON_f / DN_f
- Probability (a_f) that a detecting pattern still detects f is:

$$a_f = 1 - (1 - op)^{\frac{ON_f}{DN_f}}$$

- # of detecting patterns for a fault f is a binomial distribution, $0 < N_f < DN_f$

$$\Pr ob\{N_f = n\} = \binom{DN_f}{n} \cdot (a_f)^n \cdot (1 - a_f)^{DN_f}$$

Prediction of BCE (cont'd)

- Expectation of the BCE function for a fault *f:*

$$E[BCE_f] = \sum_{n=0}^{DN_f} (1-0.5^n) \cdot \Pr ob\{N_f = n\}$$

$$= 1-(1-0.5 \cdot a_f)^{DN_f}$$

- The predicted BCE for a given *op* is

$$BCE = \frac{1}{|F|} \sum_{f \in F} E[BCE_f]$$

Accuracy Comparison for Stuck-at-fault Coverage Prediction

ckt	obs %	0.5	0.6	0.7	0.8	0.9	0.95	Avg.
B17	sim. cov.	88.57	89.62	90.50	91.14	91.62	91.84	
	prd. cov.	88.58	89.66	90.48	91.12	91.63	91.85	
	error	0.01	0.04	0.02	0.02	0.01	0.01	0.02
s35932	sim. cov.	86.24	88.01	89.43	90.39	91.08	91.34	
	prd. cov.	86.05	88.12	89.51	90.45	91.09	91.34	
	error	0.19	0.11	0.08	0.06	0.01	0.00	0.08
s38417	sim. cov.	97.73	98.37	98.80	99.11	99.29	99.46	
	prd. cov.	97.87	98.44	98.85	99.14	99.37	99.45	
	error	0.14	0.07	0.05	0.04	0.08	0.00	0.06
s38584	sim. cov.	93.22	93.32	95.07	95.62	96.06	96.29	
	prd. cov.	93.19	94.26	95.04	95.63	96.09	96.27	
	error	0.03	0.05	0.03	0.02	0.03	0.01	0.03

Accuracy Comparison for BCE Prediction

ckt	obs %	0.5	0.6	0.7	0.8	0.9	0.95	Avg.
b17	sim. BCE	82.16	83.54	84.65	85.53	86.23	86.56	
	prd. BCE	82.46	83.79	84.75	85.60	86.29	86.59	
	error	0.30	0.25	0.10	0.07	0.06	0.03	0.02
s35932	sim. BCE	74.08	77.58	80.50	82.78	84.59	85.32	
	prd. BCE	73.90	77.71	80.59	82.82	84.59	85.33	
	error	0.18	0.13	0.09	0.04	0.00	0.01	0.08
s38417	sim. BCE	92.87	93.76	94.40	94.84	95.14	95.33	
	prd. BCE	93.18	93.97	94.53	94.93	95.22	95.33	
	error	0.31	0.21	0.13	0.09	0.08	0.00	0.14
s38584	sim. BCE	86.94	88.56	89.73	90.68	91.43	91.77	
	prd. BCE	86.94	88.53	89.75	90.70	91.46	91.78	
	error	0.00	0.03	0.02	0.02	0.03	0.01	0.02

Runtime of the Test-Quality Prediction

- Compare the runtime between our prediction scheme and a BCE fault simulation

ckt	BCE sim. (a)	20-op prd. (b)	40-op prd. (c)	(b) - (a)	(c) – (b)
b17	114.7	126.4	128.2	11.7	1.8
s35932	6.4	7.7	8.8	1.3	1.1
s38417	23.1	26.9	27.5	3.8	0.6
s38584	20.1	23.0	23.3	2.9	0.3

Outline

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  - Time compactor (MISR)
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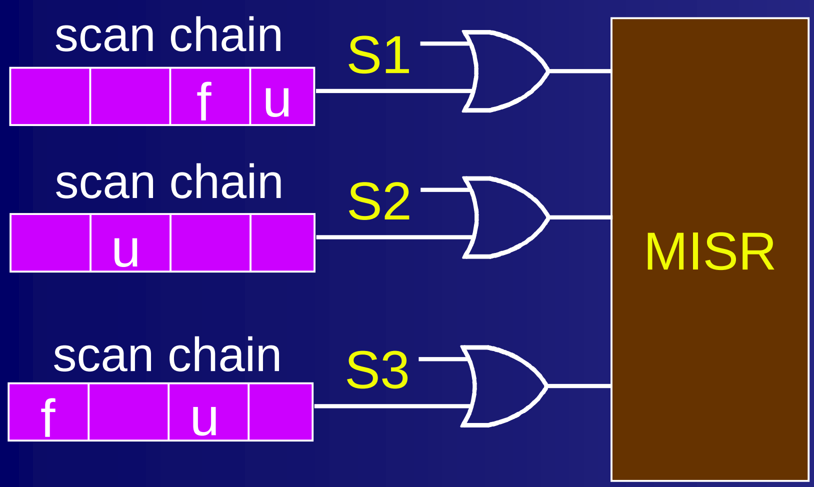
  - Diagnosis with compactor
- Design optimal space compactor
- Hybrid compaction scheme
- Conclusion

Unknown-Blocking MISR

- Block unknowns before feeding into a time compactor
- Pomeranz TCAD'04, Tang ITC'04, Chickermane ITC'04
- Required pattern-dependent blocking logic or customized ATPG
- Over-mask some useful responses



0 : must-observe
1 : blocking (for unknown)

cycle	4	3	2	1
S1	x	x	0	1
S2	x	1	x	x
S3	0	x	1	x

around 50% of the scan-out responses will be blocked !!

Coverage Loss with Different % of Observable Responses

circuit	# of pttn	# of scan FF	must-obs res. %	total tran. flt	detected tran. flt	BCE
s35932	27	2048	15.70	66316	46971	85.95
s38417	189	1742	2.44	53014	43071	95.42
s38584	191	1730	3.81	64162	48485	92.04
b17	536	1512	2.23	117998	85466	86.84

circuit	must-obs. only	observable percentage					
		50%	60%	70%	80%	90%	95%
s35932	22.77	7.37	5.23	3.46	2.06	0.92	0.44
s38417	27.14	1.76	1.22	0.75	0.43	0.20	0.11
s38584	20.66	2.46	1.76	1.01	0.63	0.28	0.13
b17	20.11	3.17	2.23	1.54	0.94	0.43	0.18
Avg.	22.67	3.69	2.61	1.69	1.02	0.46	0.22

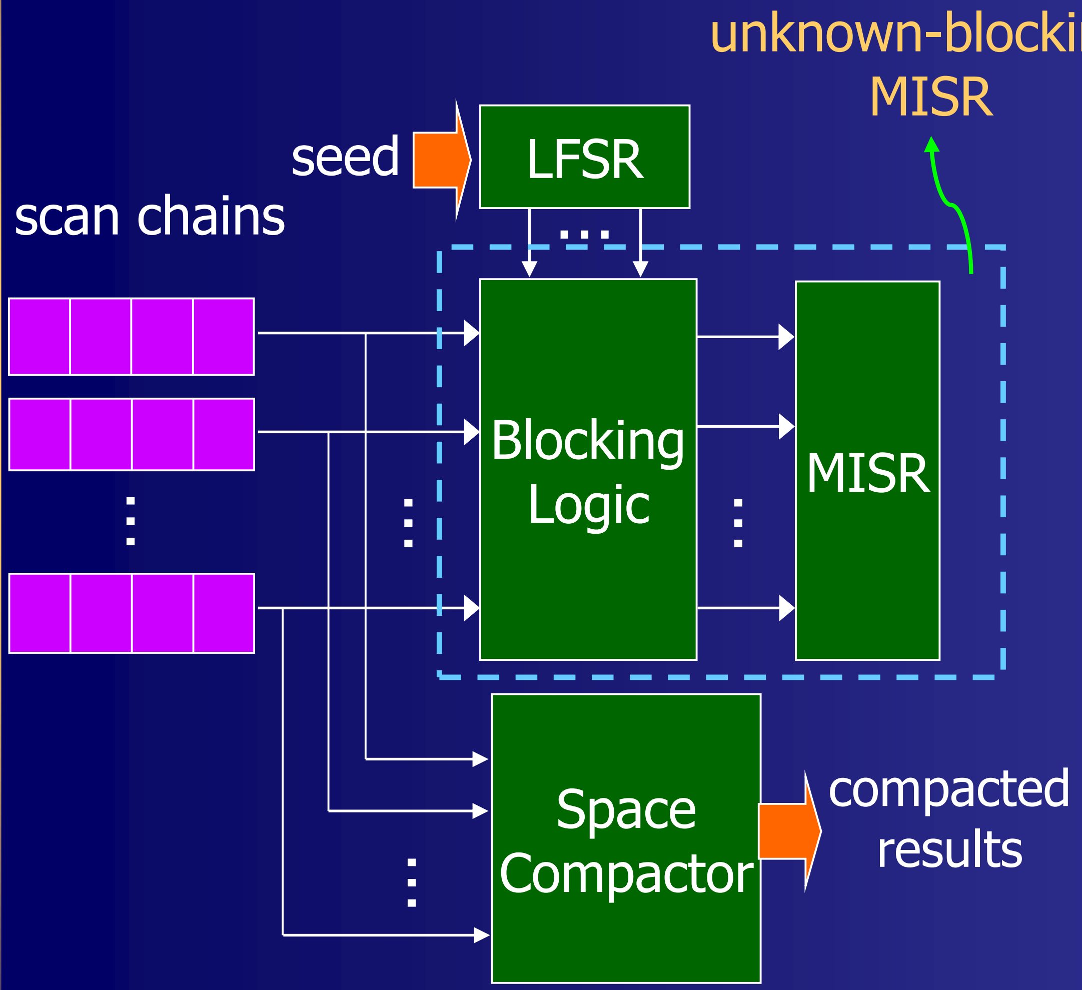
Transition fault coverage loss

Coverage Loss with Different % of Observable Responses

circuit	must-obs. only	observable percentage					
		50%	60%	70%	80%	90%	95%
s35932	18.58	5.33	2.75	2.54	1.15	0.69	0.33
s38417	22.55	0.71	0.44	0.27	0.14	0.07	0.03
s38584	20.12	2.09	1.45	0.95	0.57	0.27	0.13
b17	15.15	1.82	1.29	0.86	0.53	0.24	0.10
Avg.	19.10	2.49	1.48	1.16	0.60	0.32	0.15

BCE loss

Hybrid Compaction Scheme using Space Compactor & X-blocking MISR



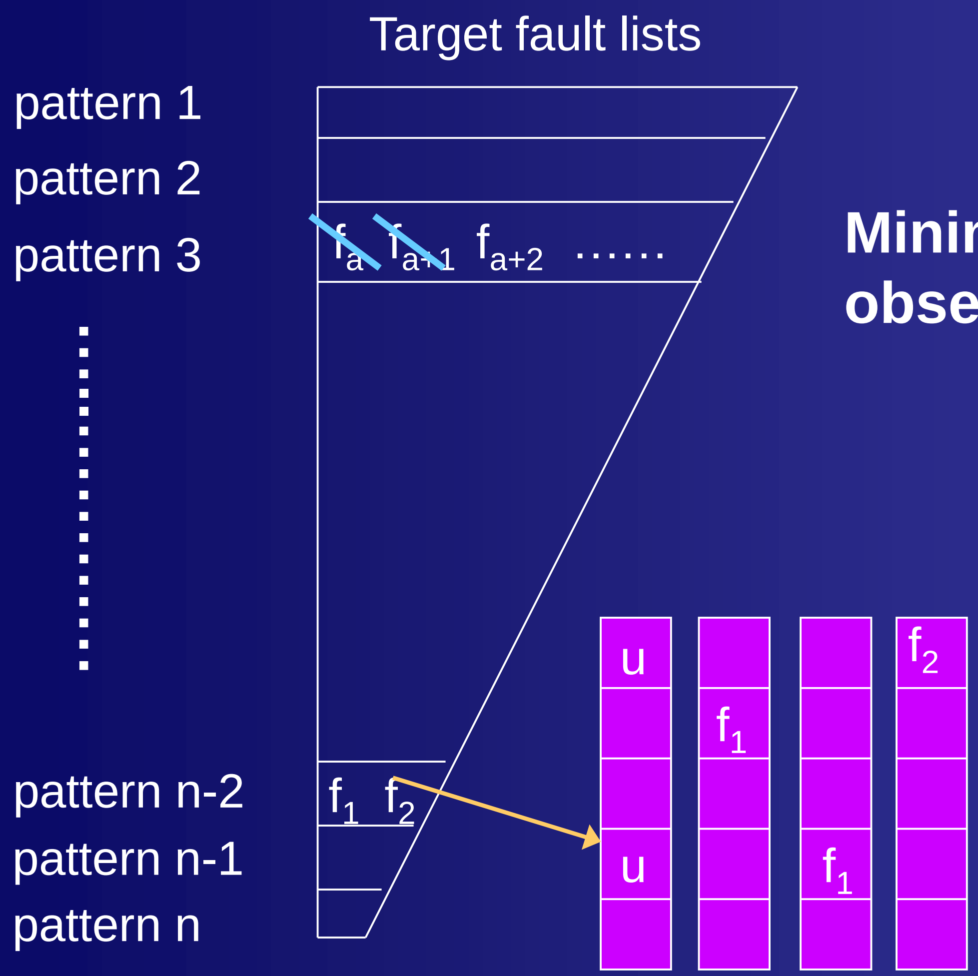
Our objective

1. ATPG-independent flow
2. Pattern-independent HW
3. Full model-fault coverage
4. Desired observable %
5. Maximal # of scan chains
6. Minimal test data

Input/Output of the Design Flow for Hybrid Compaction Scheme

- Input
  - CUT, test set, and target fault model of the test set
  - # of ATE channels (*ATE_out*) used for space compactor
  - Desired observable % for the whole compaction scheme (*target_obs_p*)
    - Desired observable % for the space compactor (*space_obs_p*)
    - *space_obs_p* = 2**target_obs_p* – 1
- Output
  - Space compactor with max number of scan chains (*max_chain*) & optimal *weight* (*w*)
  - Blocking logic for the test responses and its LFSR seeds for the control signals of the blocking logic

Reversed-order Fault Simulation for Must-observe Responses



Minimize the # of must-observe responses

Reversed-order fault simulation

Coverage and Test-Data Comparison on s35932

4 ATE channels for space compactor, 0.5% unknown, 1730 scan cells

90% desired observable percentage

	Actual obs. %	Tran. flt cov. loss (%)	BCE loss (%)
Hybrid scheme	90.67	1.45	0.96
X-blocking only	56.58	6.83	5.00

Coverage loss comparison

	Space compactor	LFSR	Total	Compaction ratio
Hybrid scheme	48	45	93	15.9
X-blocking only	_	248	248	8.3

Test data comparison

Coverage-Loss Comparison

- Hybrid compaction scheme can always achieve lower coverage loss for the un-modeled faults

		Actual obs. %	Tran. flt cov. loss (%)	BCE loss (%)
s38417	Hybrid	90.14	0.28	0.10
	X-blocking only	50.46	1.78	0.81
s38584	Hybrid	90.10	0.33	0.38
	X-blocking only	53.26	2.60	2.56
b17	Hybrid	90.39	0.51	0.14
	X-blocking only	52.78	2.87	1.75

Coverage loss comparison

Test Data Comparison

- Higher observable percentage may not require higher test data

		Space compactor	LFSR	Total	Compact ratio
s38417	Hybrid	40	30	70	24.9 X
	X-blocking only	_	32	32	54.4 X
s38584	Hybrid	40	22	62	27.9 X
	X-blocking only	_	78	78	22.2 X
b17	Hybrid	36	29	65	23.2 X
	X-blocking only	_	58	58	26.1 X

Test data comparison

Compaction Ratio for Different Unknown Percentages

- Compaction ratio of hybrid scheme increases more significantly than using X-blocking MISR, when the unknown percentage goes down

		Unknown percentage		
		0.5 %	0.3 %	0.1 %
s35932	Hybrid	22.0 x	36.6 x	41.8 x
	X-blocking only	8.3 x	8.4 x	9.2 x
s38417	Hybrid	24.9 x	39.6 x	60.1 x
	X-blocking only	54.4 x	62.2 x	72.6 x
s38584	Hybrid	27.9 x	40.2 x	64.1 x
	X-blocking only	22.2 x	22.5 x	26.6 x
b17	Hybrid	23.3 x	28.0 x	39.8 x
	X-blocking only	26.1 x	27.5 x	28.5 x

Compaction ratio comparison

Comparison to Space Compactors

Circuit	comp. ratio	method	# of channel	s.a. cov. loss (%)	tran. cov loss (%)	BCE loss (%)
s35932	22.0x	Hybrid	8	0	0.96	1.45
		X-comp	10	0.29	0.93	1.17
s38417	24.9x	Hybrid	7	0	0.10	0.28
		X-comp	10	0.17	0.38	0.33
s38584	27.9x	Hybrid	7	0	0.38	0.33
		X-comp	11	0.40	0.73	0.90
b17	23.3x	Hybrid	7	0	0.28	0.51
		X-comp	10	0.40	0.60	0.98

Experimental Results for Industrial Designs

Circuit	# of scan FFs	Gate count	# of test patterns	ATPG- detected fault
D1	4490	722K	542 (3063)	995234
D2	65560	870K	1514 (25859)	1835582

Overhead	Original area	Space comp.	X-block MISR	Total area	Overhead %	Runtime (sec)
D1	3086752	12166	16119	28285	0.92	3633
D2	3710920	12166	30017	42183	1.14	24350

Coverage loss	Actual obs. %	Tran. flt cov. loss (%)	BCE loss (%)	Compaction ratio
D1	90.92	0.06	0.05	39.3
D2	90.41	0.53	0.33	63.1

Prediction of BCE for Hybrid Compaction Scheme

- For each fault f, we collect the following statistics
  - DN_f : total # of patterns detecting fault *f* (*detecting patterns*)
  - ON_f : total # of outputs propagating a faulty value of *f* for entire test set (*faulty outputs*)
- Hybrid compaction scheme guarantee at least one detection for the stuck-at fault, N_f cannot be 0.

$$BCE = \frac{1}{F}\sum_{f \in F}(1-0.5^{N_f})$$

$$\Pr ob\{N_f = n\} = \binom{DN_f}{n} \cdot (a_f)^n \cdot (1-a_f)^{DN_f}, \; 0 < N_f < DN_f$$

Prediction of BCE for Hybrid Compaction Scheme: Lower Bound

- Because hybrid compaction scheme guarantee at least one detection for the stuck-at fault, N_f cannot be 0.

$$\Pr ob\{N_f = n\} = \binom{DN_f}{n} \bullet a_f{}^n \bullet (1-a_f)^{DN_f - n} \qquad \text{if } n>2$$

$$= DN_f \bullet a_f \bullet (1-a_f)^{DN_f - 1} + (1-a_f)^{DN_f} \qquad \text{if } n=1$$

$$BCE\_L = (1 - 0.5^{N_f})$$

$$E[BCE\_L_f] = \sum_{n=1}^{DN_f} (1-0.5^n) \bullet \Pr ob\{N_f = n\}$$

$$= 1 - (1 - 0.5 \bullet a_f)^{DN_f} + 0.5(1-a_f)^{DN_f}$$

$$BCE\_L = \frac{1}{|SF|} \sum_{f \in SF} E[BCE\_L_f]$$

Prediction of BCE for Hybrid Compaction Scheme: Upper Bound

- Detecting those undetected faults may also increase the # of detection for other faults
- $M_f = N_f + 1$, $1 < M_f < DN_f + 1$
- However, M_f cannot exceed DN_f since DN_f is the number of detecting patterns when observing all responses

$$\Pr ob\{M_f = m\} = \Pr ob\{N_f = m-1\} \bullet \frac{1}{1 - \Pr ob\{N_f = DN_f\}}$$

$$= \binom{DN_f}{m-1} \bullet a_f^{\,m-1} \bullet (1-a_f)^{DN_f - m+1} \bullet \frac{1}{1-a_f^{\,DN_f}}$$

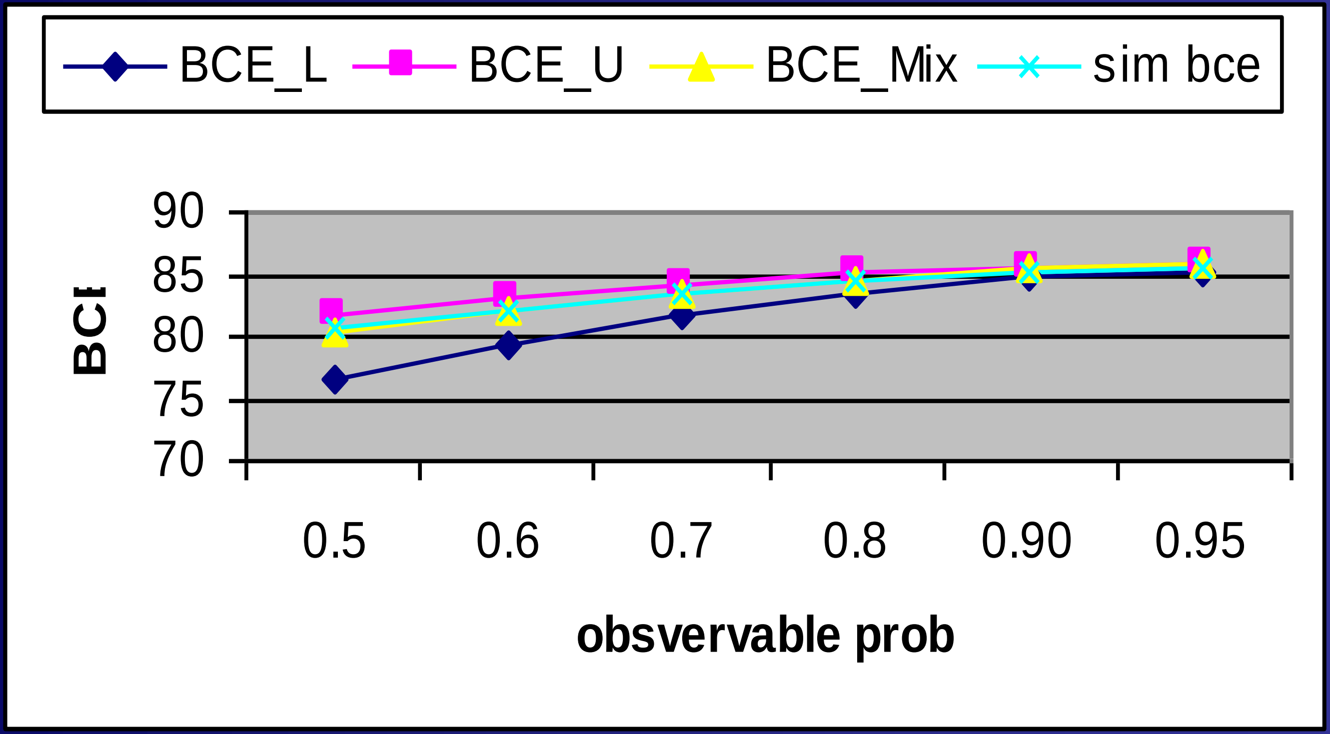
$$BCR\_U_f = (1 - 0.5^{M_f})$$

$$E[BCE\_U_f] = \sum_{m=1}^{DN_f} (1-0.5^m) \bullet \Pr ob\{M_f = m\}$$

$$= 1 - \frac{0.5}{1-a_f^{\,DN_f}} \left\{ (1-\frac{a_f}{2})^{DN_f} - (\frac{a_f}{2})^{DN_f} \right\}$$

Experimental Result for BCE Prediction

- By experiment, the actual BCE is more close to *BCE_U*
- *BCE_Mix* = 0.75 * *BCE_U* + 0.25 * *BCE_L*



BCE prediction for s35932

Conclusion

- Input-pattern compression
  - Limited by the % of specified bits
  - 1% specified bits = 100x comp. ratio
- Test-response compaction
  - Limited by % of unknowns & must-observe responses
  - 1% unknown < 100x comp. ratio
- Speedup of test-application time may not be as same as data compression ratio
- All compression/compaction tool are bundled with ATPG tool
- Diagnosis with compactor? No!